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Master's Thesis

Thermo-mechanical analysis of Cu-Sn alloy-Cu flipchip bonding and via interface in TSV structure

Graduate School of Chosun University

Department of Naval Architecture and Ocean Engineering

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ABSTRACT

TSV구조의 Via계면과 Cu-Sn 합금-Cu 플립칩 접합부의 열에 의한 역학적 특성 평가

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모바일과 유비쿼터스 센서 네트워크 센서 시대가 도래함에 따라 가볍고, 작고, 얇고, 멀티기능을 구현할 수 있는 부품에 대한 요구가 증대하고 있다. 이에 대한 여러 가지 솔루션 중 MCM(Multi Chip Module)의 개념을 수직 방향으로 확장시킨 3D IC가 최근 각광을 받고 있다. 이는 물리적인 한계에 부딪힌 반도체 집적 공정의 한계를 극복하여 지속적으로 무어의 법칙에 맞춰 집적도를 향상시킬 수 있을 뿐만 아니라 소재와 공정이 달라도 3차원적으로 집적이 가능하여 메모리와 프로세서로 대표되는 디지털 칩뿐만 아니라 아날로그/RF, 수동소자, 전력소자, 센서/액추에이터, 바이오칩 등을 하나로 패키징할 수 있는 장점이 있기 때문이다.

솔더 접합 기술인 Flip chip packaging 기술은 한 개의 chip내에 1000개 이상의 I/O를 구현 할 수 있어 현대 각광을 받는 패키징 기술이다. 또한 Si 웨이퍼에 구멍을 뚫어 Chip들을 위로 쌓아 올리면서 한층 한층씩 접합을 시키는 MCP(Multi Chip Packaging)는 고집적, 고밀도의 패키징 기술의 하나로써 I/O의 개수를 더욱 많이 구현할 수 있다는 장점이 있다. MCP 기술 중 TSV(Through Via Hole)의 구조는 Si 웨이퍼에 구멍을 뚫어 연결하는 방법으로 위로 쌓아올린 칩들을 직접 연결할 수 있어 다른 방법에 비해 보다 작은 접합면적에서 많은 기능을 실행할 수 있다. 이러한 기술을 시행하기 위해서는 미세 솔더 범프를 필요로 한다.

본 연구에서는 MCP 방법 중 하나인 TSV구조에서의 플립칩 접합기술을 이용 할 때 장치의 디자인의 변화에 따른 열응력분포를 확인하여 신뢰성을 평가하고자 하고, 시뮬레이션 변수를 TSV 직경, 솔더 두께, TSV 피치, 언더필 두께로 선택하여 솔더계면과 비아계면에서의 열 하중에 의해 발생하는 열응력들을 분석하여 신뢰성을 평가하고자 한다. 열응력값에 대한 해석은 Abaqus/CAE 프로그램을 이용하였고, 신뢰성의 평가는 Minitab16을 이용하여 Taguchi 직교 9배열법에 의해 81번의 계산 통하여 각각의 변수에 대한 열응력의 결과값으로 신뢰성을 평가하였다.

Chapter 1
Introduction

1.1 Research Purpose and method

3D packaging has been the focus of many recent studies and researches since it possesses many advantages over the traditional 2D packaging such as: (1) better form factor (size miniaturization to increase density and capacity/volume ratio), (2) integration of heterogeneous functions in a single package (e.g. processor, logic, application specific integrated circuits (ASIC) and memory), (3) utilizing short vertical interconnects instead of long 2D interconnects to increase electrical performance level, (4) parallel processing, (5) low power consumption, (6) lower cost/GB or cost/GH ratio. However, in order for this technology to be used in high volume production of electronic devices, many issues such as reliability, quality and manufacturability must be resolved and technologies compatible with existing technologies and processes of IC fabrication should be identified and studied.

Three-dimensional integrated circuit (3D IC) is a promising technology in today's IC packaging industry. Since the technology is in infancy stages, many aspects of this technology are still under heavy investigation. Reliability of through silicon via (TSV) interconnects and interlayer bondings between the silicon layers are issues that become more complicated in 3D ICs due to the complexity of the architecture and miniaturized interconnect. Optimizing design of these devices is essential in order to avoid short fatigue life of interconnects. This manuscript addresses the impact of design parameters such as solder thickness, TSV diameter and pitch, and

underfill thickness and properties on thermo-mechanical durability of direct chip attach (DCA) solder joints and TSV interconnects used in a 3D IC packages. A design was proposed where DCA is used to connect four layers of ICs and TSVs are used to connect the active layer of the dies to the second silicon layer.

A numerical experiment is designed to vary these factors at three levels using L9 orthogonal array. A 3-dimensional model of the package was built and model was solved under an accelerated thermal cycle loading. Solder is considered to be elasto-plastic material and copper interconnects are assumed to follow bi-linear isotropic hardening behavior. Minitab software was used to analyze the result of experiment.

chapter 2
Theoretical background

2.1 Principles of Flip Chip Bonding (FCB)

2.1.1 Principles of FCB

Flip chip micro electronic assembly is the direct electrical connection of face-down (hence, "flipped") electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. In contrast, wire bonding, the older technology which flip chip is replacing, uses face-up chips with a wire connection to each pad.

Flip chip components are predominantly semiconductor devices; however, components such as passive filters, detector arrays, and MEMs devices are also beginning to be used in flip chip form. Flip chip is also called Direct Chip Attach (DCA), a more descriptive term, since the chip is directly attached to the substrate, board, or carrier by the conductive bumps.

IBM introduced flip chip interconnection in the early sixties for their mainframe computers, and has continued to use flip chip since then. Delco Electronics developed flip chip for automotive applications in the seventies. Delphi Delco currently places over 300,000 flip chip die per day into automotive electronics. Most electronic watches, and a growing percentage of cellular phones, pagers, and high speed microprocessors are assembled with flip chip.

Worldwide flip chip consumption is over 600,000 units per year, with a projected annual growth rate of nearly 50% per year. Semiconductor manufacturers currently bump for flip chip assembly about 3% of wafers

produced, and are expected to be bumping 10% within a few years.

Fig. 2.1 Wire-Bonding VS Flip-Chip Bonding

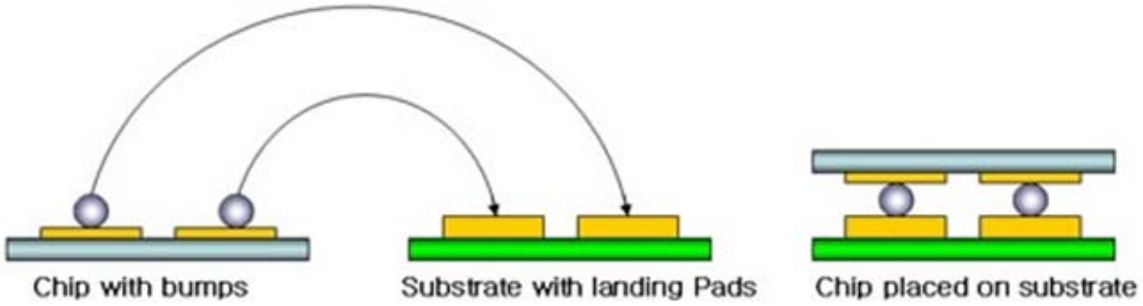


Fig. 2.2 Flip-chip process structure

Next scribes is fundamental flip chip process.

① Build up bump at chip substrate.

② "face-down" Bumped chip by substrate.

③ Filling the empty space of between chip and substrate by underfill process.

2.1.2 Characteristics and process of FCB

There are three stages in making flip chip assemblies: bumping the die or wafer, attaching the bumped die to the board or substrate, and, in most cases, filling the remaining space under the die with an electrically non-conductive material. The conductive bump, the attachment materials, and the processes used differentiate the various kinds of flip chip assemblies. The following sections describe the most

common bumping and attaching methods. The cost, performance, and space constraints of the application determine which method best suits it.

Bump Requirements

The bump serves several functions in the flip chip assembly. Electrically, the bump provides the conductive path from chip to substrate. The bump also provides a thermally conductive path to carry heat from the chip to the substrate. In addition, the bump provides part of the mechanical mounting of the die to the substrate. Finally, the bump provides a spacer, preventing electrical contact between the chip and substrate conductors, and acting as a short lead to relieve mechanical strain between board and substrate.

(a) Solder Bump Flip Chip

The solder bumping process first requires that an under bump metallization (UBM) be placed on the chip bond pads, by sputtering, plating, or other means, to replace the insulating aluminum oxide layer and to define and limit the solder-wetted area. Solder is deposited over the UBM by evaporation, electroplating, screen printing solder paste, or needle-depositing.

After solder bumping, the wafer is sawn into bumped die. The bumped die are placed on the substrate pads, and the assembly is heated to make a solder connection. Solder bumped die and wafers, and assembly services are available from several suppliers.

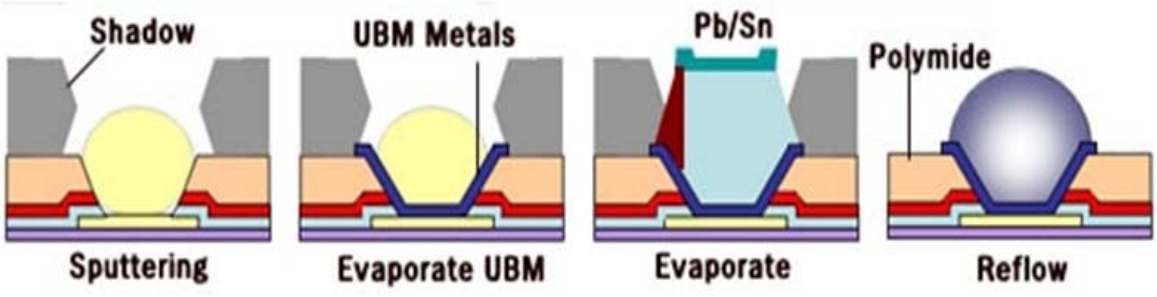


Fig. 2.3 Evaporated bump process

(b) Plated Bump Flip Chip

Plated bump flip chip uses wet chemical processes to remove the aluminum oxide and plate conductive metal bumps onto the wafer bond pads. Plated nickel-gold bumps are formed on the semiconductor wafer by electroless nickel plating of the aluminum bond pads of the chips. After plating the desired thickness of nickel, an immersion gold layer is added for protection, and the wafer is sawn into bumped die. Attachment generally is by solder or adhesive, which may be applied to the bumps or the substrate bond pads by various techniques. Plated bump die, and assembly services, are available from several suppliers.

(c) Stud Bump Flip Chip

The gold stud bump flip chip process bumps die by a modified standard wire bonding technique. This technique makes a gold ball for wire bonding by melting the end of a gold wire to form a sphere. The gold ball is attached to the chip bond pad as the first part of a wire bond. To form gold bumps instead of wire bonds, wire bonders are modified to break off the wire after attaching the ball to the chip bond pad. The gold ball, or "stud bump" remaining on the bond pad provides a permanent connection through the aluminum oxide to the underlying metal.

The gold stud bump process is unique in being readily applied to individual single die or to wafers. Gold stud bump flip chips may be attached to the substrate bond pads with adhesive or by thermosonic gold-to-gold connection. Die bumping and assembly services are available from several suppliers.

(d) Adhesive Bump Flip Chip

The adhesive bump flip chip process stencils conductive adhesive to form bumps on an under-bump metal. The cured adhesive acts as bumps. Attachment is by an additional layer of conductive adhesive. Adhesive bumping and assembly is available from licensed suppliers.

(e) Flip Chip Underfill

As described above, one function of the bump is to provide a space between the chip and the board. In the final stage of assembly, this under-chip space is usually filled with a non-conductive "underfill" adhesive joining the entire surface of the chip to the substrate.
The underfill protects the bumps from moisture or other environmental hazards, and provides additional mechanical strength to the assembly. However, its most important purpose is to compensate for any thermal expansion difference between the chip and the substrate. Underfill mechanically "locks together" chip and substrate so that differences in thermal expansion do not break or damage the electrical connection of the bumps.

Underfill may be needle-dispensed along the edges of each chip. It is drawn into the under-chip space by capillary action, and heat-cured to form a permanent bond.

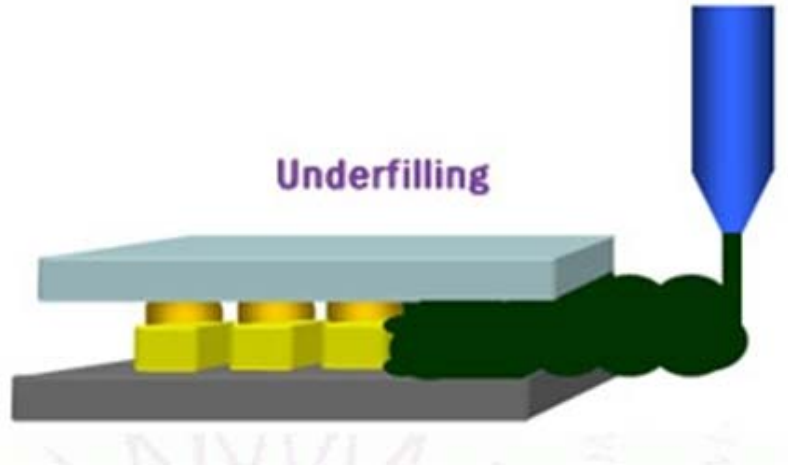


Fig. 2.4 Underfilling Process

2.2 Principles and characteristics of TSV

2.2.1 Principles of TSV

Semiconductor integration technology has been widely spread in two-dimensional applications over the past three decades. This wide application has been employed not only in the field of the electronics industries but also in a lot of related industries such as optoelectronics, bioelectronics, medical systems, electronics analysis, computer systems, military systems, satellite systems, submarine systems, and so on. From the consumer area to ultra-high-end products and military usage, almost all industrial products incorpo-rate semiconductor devices. One significant reason for this rapid progress is the good scalability of metal-oxide-semiconductor (MOS) devices. But recently the actual device has begun to deviate from the ideal scaling theory. The main cause is difficulty of operation voltage scaling. The value of kT/q does not scale down, and thus lowering threshold voltage (Vth) of an MOS transistor is difficult without increasing subthreshold leakage. Without Vth scaling, power and performance became a tradeoff.

Under this circumstance, in order to bring out high performance from LSI chips while restricting their power, there are two approaches. One is reconsidering circuits and system architecture from view point of power consumption. Another is concerning LSI structure. In recent devices, the signal propagation delay is mainly determined by wiring length and pin capacitance. Three-dimensional large-scale integration (3D-LSI) is the one solution to improve performance without increase of power consumption. One of the key issues to realize 3D-LSI is the method of information transfer and the supply of electric power among stacked chips. There are many methods to connect interchip, such as wire-bonding, edge connect, capacitive or inductive coupling method, and direct contact using through-silicon via (TSV).

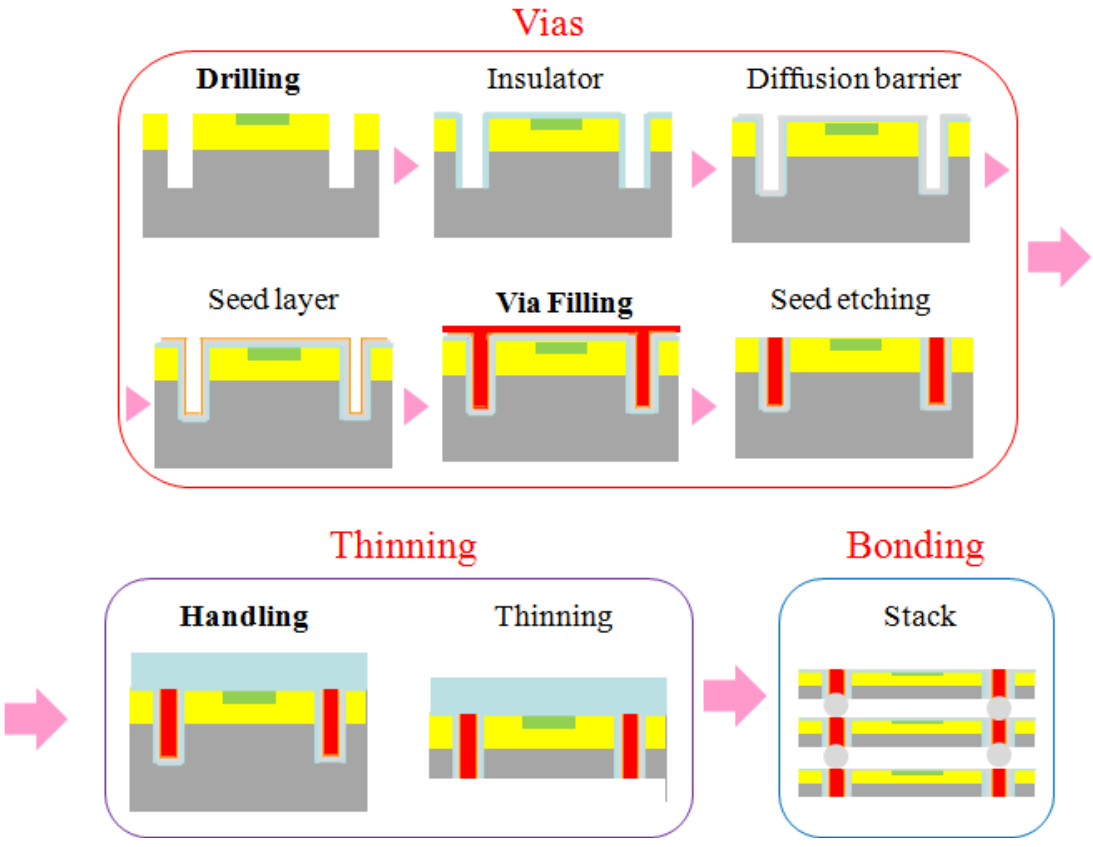


Fig. 2.5 3D TSV process

2.2.2 Characteristics and process of TSV

Through Silicon Via (TSV) is an enabling technology that allows electrical connections to be formed through a silicon wafer or multi-wafer devices. Electrical connections through a silicon wafer allow for reduced die footprints and interlayer connectivity. When combined with Wafer Level Packaging (WLP), TSVs minimize die size, allow conventional or flip-chip bonding, and help minimize cost of the final macroscale device.

Fig. 2.6 Example of TSV functions

Connections between layers are created through etching via holes, selectively insulating, and filling with conductive polysilicon. This platform includes deep etched silicon trenches, isolation or grounding vias, polysilicon filling, and the option for integration in SOI wafer

stacks. Including aspect ratio, thickness, pitch, resistivity, capacitance, geometry, and isolation resistance.

• Improved Performance: closer positioning of the dies on the substrate and shorter interconnection lengths should enhance system speed dramatically.

• Higher Integration Density: substituting several packages for one slightly larger but single package, should either free board real estate for other use or help reduce the board size.

• Lower Power Consumption: smaller drivers are needed resulting in lower power consumption.

• Mixed Signal Applications: MCP allows the integration of chips made from different technologies in one package.

• Lower Cost: cost savings result from fewer packages with a fewer number of leads, a simplified board layout ,and the feasibility of mixed technologies in the same package. Smaller risks are associated with MCPs compared to MCMs since existing package and board assembly equipment and technologies are used. For instance, the same CAD design software for board layout can be extended to MCP substrate design, standard pick-and-place tooling can be used for die placement, the same lead frame outline can be applied eliminating the needs for new molds or trim and form tooling, and test sockets and even shipping containers for MCPs fitting the form factor of single chip packages can be readily deployed.

• Time-to-Market: inserting several dies into the same package allows much faster introduction of the product into the market compared to integrating all the desired functions on a new single chip. The latter can still be achieved provided that the product needs and volume forecasted are warranted. Thus, MCP finds a special niche in packaging, acting as transitory stage between product needs and chip integration. The timely introduction is most important since the highest profit margins are always achieved in the early stages of the product life cycle.

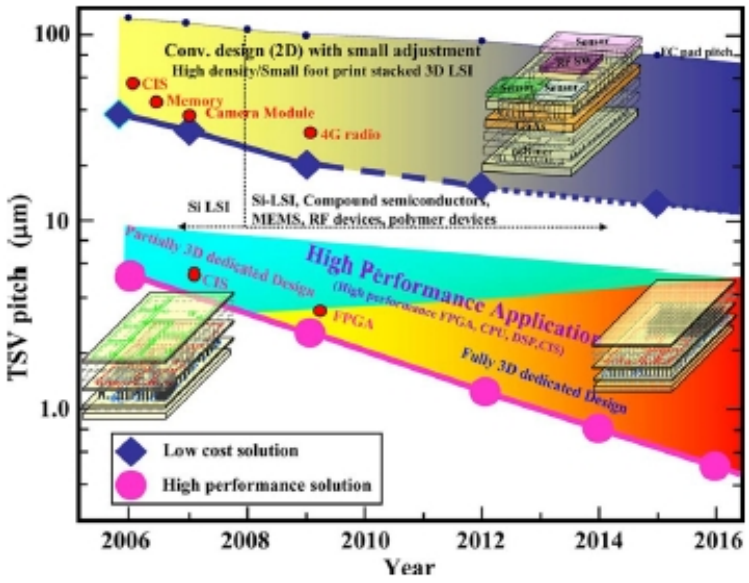


Fig. 2.7 TSV for 3D technology road map.

2.3 Characteristic of lead free solder materials

In the 1990's, a problem was revealed that lead (Pb) contained in soldering materials (such as Sn-Pb) of waste electronic components was melted away by acid rain and contaminated groundwater. Since then, the study of lead-free solder has been pursued. Since the year 2000, under the leadership of major electrical machinery manufacturers, lead-free solder has begun to be put into practical use. The use of lead-free solder has become mainstream due to the increasing global trend in environmental issues such as the RoHS directive (the restriction on the use of hazardous substances which will be enforced by the European Union starting July 1, 2006).

(a) Sn-Ag

In addition to liquid and the two terminal solution phases, (Ag) and (Sn), this system has two intermediate phases, (ζAg) and Ag_3Sn. Both intermediate phases form by peritectic reactions. The eutectic reaction in which liquid with X_{Sn}=0.965 decomposes into Ag_3Sn and (Sn) at a temperature of 221℃ is well established. The two available thermodynamic assessments give very similar results. Moon et al. pointed out that in both assessments, the liquidus for primary Ag_3Sn formation needs further refinement. (see Fig. 2.8)

(b) Sn-Zn

The phase diagram of this system is relatively well established and a number of thermodynamic assessments asr available for this simple eutectic system. At 198.5℃, the liquid decomposes into the two terminal solid solutions, (Zn) and (Sn). However, the composition reported for the liquid phase at the eutectic temperature varies between X_{Sn}= 0.906 and X_{Sn}= 0.921. (see Fig. 2.8)

(c) Sn-Sb

In addition to liquid and the two terminal solution phases, (Sb) and (Sn), this system has two intermediate phases, SbSn (β) and Sb_3Sn_2. Both intermediate phases, as well as (Sn), from by peritectic reaction forming (Sn) occurs at a temperature of 250℃. The two available thermodynamic assessment are based on the experimental work of Predel and Schwermann. (see Fig. 2.8)

(d) Sn-In

In addition to liquid and the two terminal solution phase (In) and (Sn), this system has two intermediate phases, β and ϒ. Both intermediate phases from the liquid and one of the terminal solution phases. At a temperature of 120℃, the liquid with X_{Sn}=0.491 decomposes into the two intermediate phases. The evaluation by Okamoto concludes that most of the boundaries of the solid phases need to be better estabilised for concentrations with $X_{Sn} \geq 0.75$. The two themodynamic assessments available are based on the evalution by Okamoto. (see Fig. 2.8)

(e) Sn-Cu

In addition to liquid and the two terminal solution phases, (Cu) and (Sn), this system has seven intermediate phases, β , ϒ, $Cu_{41}Sn_{11}$ (δ), $Cu_{10}Sn_3$ (ζ), Cu_3Sn (γ), and Cu_6Sn_5/Cu_6Sn_5, (η/η^1, high- and low-temperature forms). All of the intermediate phases form by peritectic or peritectoid reactions. All of the copper-rich intermediate phases decompose in eutectoid reactions at temperatures above 350℃ and, therefore, only the Cu_3Sn and Cu_6Sn_5/Cu_6Sn_5' phases are of interest for solder applications. The temperature of 227℃ for the eutectic reaction, where liquid phase, either X_{Sn}= 0.91 or X_{Sn}=

0.93. Moon et al. showed that the composition of X_{Sn}= 0.91 is consistent with the eutectic temperature and the slope of the liquidus for primary (Sn) formation. The two available thermodynamic assessments give very similar results. Moon et al. pointed out that the liquidus for primary Cu_6Sn_5 formation needs further refinement. (see Fig. 2.8)

(f) Sn-Bi

Most parts of the phase diagram of this simple eutectic system are well established. At 138℃, the liquid with X_{Sn}=0.43 decomposes into the two terminal solid solutions, (Bi) and (Sn). However, the solubility limit of tin in (Bi) is not reliably known although a lower value is preferred. Lee etal. accepted this lower value for the (Bi) homegeneity range and also used experimental data of the Sn-Bi-In system for the refinement of the description of the Sn-Bi system. (see Fig. 2.8)

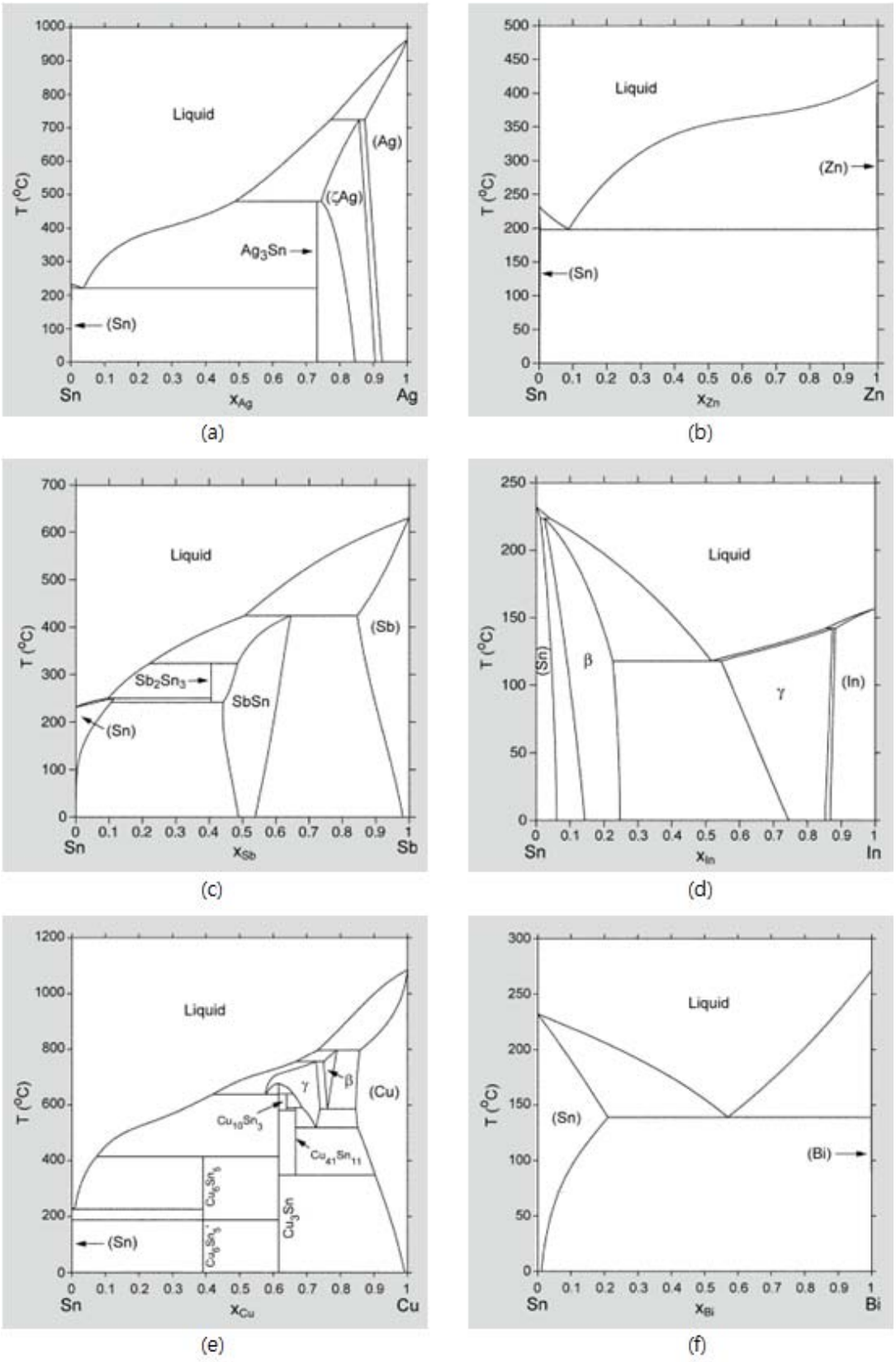


Fig. 2.8 The calculated phase diagram of lead free solders

Chapter 3
Thermal elasto-plastic theory

3.1 Theory of thermal convection analysis

The Abaqus/Standard capability for uncoupled heat transfer analysis is intended to model solid body heat conduction with general, temperature-dependent conductivity; internal energy (including latent heat effects); and quite general convection and radiation boundary conditions. This section describes the basic energy balance, constitutive models, boundary conditions, finite element discretization, and time integration procedures used.

(a) Energy balance

The basic energy balance is (Green and Naghdi)

$$\int_V \rho \dot{U}\, dV = \int_S q\, dS + \int_V r\, dV \qquad (3.1)$$

where V is a volume of solid material, with surface area S; ρ is the density of the material; $\dot{U}$ is the material time rate of the internal energy; q is the heat flux per unit area of the body, flowing into the body; and r is the heat supplied externally into the body per unit volume. It is assumed that the thermal and mechanical problems are uncoupled in the sense that $U = U(\theta)$ only, where θ is the temperature of the material, and q and r do not depend on the strains or displacements of the body. For simplicity a Lagrangian description is assumed, so "volume" and "surface" mean the volume and surface in the reference configuration.

(b) Constitutive definition

This relationship is usually written in terms of a specific heat, neglecting coupling between mechanical and thermal problems:

$$c(\theta) = \frac{dU}{d\theta}$$

except for latent heat effects at phase changes, which are given separately in terms of solidus and liquidus temperatures (the lower and upper temperature bounds of the phase change range) and the total internal energy associated with the phase change, called the latent heat. When latent heat is given, it is assumed to be in addition to the specific heat effect (see Fig. 3.1).

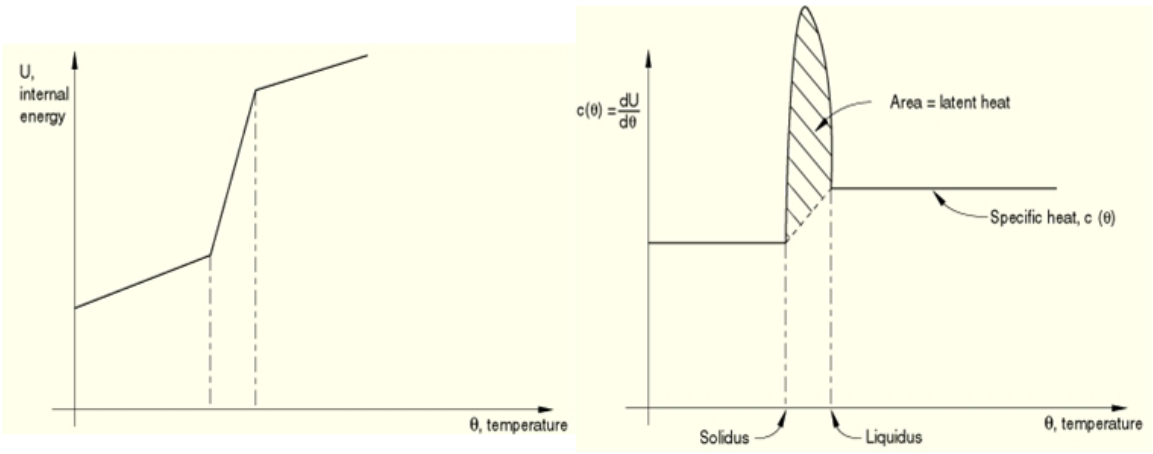


Fig. 3.1 Specific heat, latent heat definition

For many cases it is reasonable to assume that the phase change occurs within a known temperature range, which can be specified by the user. However, in some cases it may be necessary to include a kinetic theory for the phase change to model the effect accurately (an example would be the prediction of crystallization in a polymer casting process). For such cases the user can model the process in considerable detail, using the solution-dependent state variable feature in Abaqus/CAE.

Heat conduction is assumed to be governed by the Fourier law,

$$f = -k\frac{\partial\theta}{\partial x} \qquad (3.2)$$

where k is the conductivity matrix, $k = k(\theta)$; f is the heat flux; and x is position. The conductivity k can be fully anisotropic, orthotropic, or isotropic.

(c) Spatial discretization

A variational statement of the energy balance, Equation 3.1, together with the Fourier law, Equation 3.2, is obtained directly by the standard Galerkin approach as

$$\int_V \rho\dot{U}\,\delta\theta\,dV + \int_V \frac{\partial\delta\theta}{\partial\delta x}\cdot k\cdot\frac{\partial\theta}{\partial x} = \int_V \delta\theta\, r\, dV + \int_{sq} \delta\theta\, q\, dS \qquad (3.3)$$

where $\delta\theta$ is an arbitrary variational field satisfying the essential boundary conditions. The body is approximated geometrically with finite elements, so the temperature is interpolated as

$$\theta = N^N(x)\theta^N,\ \ N = 1, 2, \ldots,$$

where θ^N are nodal temperatures. The Galerkin approach assumes that $\delta\theta$, the variational field, is interpolated by the same functions:

$$\delta\theta = N^N\delta\theta^N$$

First- and second-order polynomials in one, two, and three dimensions are used for the N^N. With these interpolations the variational

statement, Equation 3.3, becomes

$$\delta\theta^N \int_V N^N \rho \dot{U}\, dV + \int_V \frac{\partial N^N}{\partial x} \cdot k \cdot \frac{\partial \theta}{\partial x} dV = \int_V N^N r\, dV + \int_{sq} N^N q dS$$

and since the $\delta\theta^N$ are arbitrarily chosen, this gives the system of equations

$$\int_V N^N \rho U dV + \int_V \frac{\partial N^N}{\partial x} \cdot k \cdot \frac{\partial \theta}{\partial x} dV = \int_V N^N r dV + \int_{sq} N^N q dS \qquad (3.4)$$

This set of equations is the "continuous time description" of the geometric approximation.

(d) Time integration

Abaqus/Standard uses the backward difference algorithm:

$$\dot{U}_{t+\Delta t} = (U_{t+\Delta t} - U_t)(1/\Delta t) \qquad (3.5)$$

This operator is chosen for a number of reasons. First of all, we choose from one-step operators of the form

$$f_{t+\Delta t} = f_t + ((1-\gamma)\dot{f}_t + \gamma \dot{f}_{t+\Delta t})\Delta t$$

because of their simplicity in implementation (for example, no special starting procedures are needed) and well-understood behavior. For such $\gamma < 1/2$ operators are only conditionally stable for linear heat transfer problems. We prefer to work with unconditionally stable methods, because Abaqus is most commonly applied to problems where the

solution is sought over very long time periods (compared to the stability limit for the explicit form of the operator, $\gamma = 0$), and so choose $\gamma \geq 1/2$. Of these operators the central difference method, $\gamma = 1/2$, has the highest accuracy. However, that form of the operator tends to produce oscillations in the early time solution that are not present in the backward difference form. Thus, we use $\gamma = 1$: backward difference. Introducing the operator, Equation 3.5, into the energy balance Equation 3.4 gives

$$\frac{1}{\Delta t}\int_V N^N \rho(U_{t+\Delta t})dV + \int_V \frac{\partial N^N}{\partial x}\cdot k \cdot \frac{\partial \theta}{\partial x}dV \qquad (3.6)$$

$$-\int_V N^N r\,dV - \int_{sq} N^N q\,dS = 0$$

This nonlinear system is solved by a modified Newton method. The method is modified Newton because the tangent matrix (the Jacobian matrix) that is, the rate of change of the left-hand side of Equation 3.6 with respect to ${\theta^N}_{t+\Delta t}$ is not formed exactly. The formation of the terms in this tangent matrix is now described.

The internal energy term gives a Jacobian contribution:

$$\frac{1}{\Delta t}\int_V N^N \rho \frac{dU}{d\theta}|_{t+\Delta t}\, N^M dV$$

$(dU/d\theta)|_{t+\Delta t}$ is the specific heat, $c(\theta)$, outside the latent heat range, and is $c + L/(\theta_L - \theta_S)$ if $\theta_L > \theta_{t+\Delta t} > \theta_S$ at the integration point, where and θ_L are θ_S the liquidus and solidus temperatures and L is the latent heat associated with this phase change.

In severe latent heat cases this term can result in numerical instabilities, as the stiffness term $dU/d\theta$ is small outside the

solidus-liquidus temperature range and is very stiff inside that rather narrow range. To avoid such instabilities in those cases this term is modified to a secant term during the early iterations of the solution to a time step. Since the modification occurs only in cases involving latent heat, it affects only those problems.
The conductivity term gives a Jacobian contribution:

$$\int_V \frac{\partial N^N}{\partial x} \cdot k\,|_{t+\Delta t} \cdot \frac{\partial N^M}{\partial x} + \int_V \frac{\partial N^N}{\partial x} \cdot \frac{\partial k}{\partial \theta}|_{t+\Delta t} \cdot \frac{\partial \theta}{\partial x}|_{t+\Delta t} N^M dV$$

The second of these terms is typically small, since the conductivity usually varies only slowly with temperature. Because of this, and because the term is not symmetric, it is usually more efficient to omit it. This term is omitted unless the unsymmetric solver is chosen. Prescribed surface fluxes and body fluxes can also be temperature dependent and will then give rise to Jacobian contributions.
With film and radiation conditions, the surface flux term gives a Jacobian contribution:

$$\int_S N^N \frac{\partial q}{\partial \theta}|_{t+\Delta t} N^M dS$$

For film conditions, $q = h(\theta)(\theta - \theta^o)$

$$\frac{\partial q}{\partial \theta} = \frac{\partial h}{\partial \theta}(\theta - \theta^o) + h$$

while for radiation, $q = A(\theta^4 - \theta^{o4})$

$$\frac{\partial q}{\partial \theta} = 4A\theta^3$$

These terms are included in exactly this form in the Jacobian. The modified Newton method is then

$$[\frac{1}{\Delta t}\int_V N^N \rho \frac{dU}{d\theta}|_{t+\Delta t} N^M dV + \int_V \frac{\partial N^N}{\partial x}\cdot k|_{t+\Delta t}\cdot \frac{\partial N^M}{\partial x} dV \qquad (3.7)$$

$$+ \int_s N^N (\frac{\partial h}{\partial \theta}(\theta - \theta^o) + h + 4A\theta^3) N^M dS] c^{-M}$$

$$= \int_V N^N r\, dV + \int_{sq} N^N q\, dS - \frac{1}{\Delta t}\int_V N^N \rho (U_{t+\Delta t} - U_t)\, dV$$

$$- \int_V \frac{\partial N^N}{\partial x}\cdot k \cdot \frac{\partial \theta}{\partial x} dV$$

$with\ \theta^N_{t+\Delta t, i+1} = \theta_{t+\Delta t}$

i = iteration number

For purely linear systems Equation 3.7 is linear in c^{-M} and, hence, in $\theta^N_{t+\Delta t}$, so a single equation solution provides the $\theta^N_{t+\Delta t}$. Since the method usually is only a minor modification of Newton's method, convergence is rapid. Abaqus/Standard uses an automatic (self-adaptive) time stepping algorithm to choose Δt. This is based on a user-supplied tolerance on the maximum temperature change allowed in a time increment, and the increment is adjusted according to this parameter, as well as the convergence rate of Equation 3.7 in nonlinear cases.

The first-order heat transfer elements (such as 2-node link, 4-node quadrilateral, and 8-node brick) use a numerical integration rule with the integration stations located at the corners of the element for the heat capacitance terms. This means that the Jacobian term associated with the internal energy rate is diagonal. This approach is especially effective when strong latent heat effects are present. The second-order elements use conventional Gaussian integration. Thus, second-order

elements are to be preferred for problems when the solution will be smooth (without latent heat effects), whereas the first-order elements should be used in nonsmooth cases (with latent heat). The HEATCAP element is available for modeling lumped heat capacitance at a point. The associated concentrated film and concentrated radiation loading options are specified by the user. These loading options are also allowed in coupled temperature-displacement and coupled thermal-electrical analysis.

3.2 Theory of thermal elasto-plastic analysis

In the thermal elastic problem, basic equations such as 1) Equilibrium equation, 2) Equation of strain-displacement relation and 3) Equation of stress-strain relation are needed to solve the problem. 1) Equilibrium equation can be replaced by principle of virtual work. These equations, 1) Principle of virtual work, 2) Equation of strain-displacement relation and 3) Equation of stress-strain relation are used in finite element method as the basic equations. Each equation is given in matrix form as follows:

$$\int_V \delta\{\varepsilon\}^T\{\sigma\}dV - \int_V \delta\{U\}^T\{\overline{F}\}dV - \int_{S_\sigma} \delta\{U\}^T\{\overline{T}\}dS = 0 \qquad (3.8)$$

where $\{\sigma\}$: stress vector, $\{\varepsilon\}$:strain vector, $\{U\}$:displacement vector, $\{\overline{F}\}$:body force vector per unit volume, $\{\overline{T}\}$:surface force vector per unit area, V :volume of an object, and S_σ : area given mechanical boundary condition.

$$\{\varepsilon\} = [A]\{U\} \qquad (3.9)$$

where matrix $[A]$ includes the differential operator.

$$\{\varepsilon\} = \{\varepsilon^e\} + \{\varepsilon^T\} \qquad (3.10)$$

where $\{\varepsilon\}$:total strain vector, $\{\varepsilon^e\}$:elastic strain vector and $\{\varepsilon^T\}$:thermal strain vector.

$$\{\sigma\} = [D^e]\{\varepsilon^e\} \qquad (3.11)$$

where $[D^e]$ is elastic stress-strain matrix. From the equation (3.10) and (3.11), an equation of stress-strain relation is obtained as follows.

$$\{\sigma\} = [D^e](\{\varepsilon^e\} - \{\varepsilon^T\}) \qquad (3.12)$$

$$[k]\{d\} = \{f_s\} + \{f_v\} + \{f_T\} \qquad (3.13)$$

where $[k]$:stiffness matrix of element, $\{f_s\}$:nodal force vector due to surface force, $\{f_v\}$:nodal force vector due to body force and $\{f_T\}$:pseudo nodal force vector due to thermal strain. These are

consisted as bellows.

$$[k] = \int_{V^e} [B]^T [D^e][B] dV \{d\} \tag{3.14}$$

$$\{f_s\} = \int_{S_\sigma^e} [N]^T \{\overline{T}\} dS \tag{3.15}$$

$$\{f_v\} = \int_{V^e} [N]^T \{\overline{F}\} dV \tag{3.16}$$

$$\{f_T\} = \int_{V^e} [B]^T [D^e] \{\varepsilon^T\} dV \tag{3.17}$$

Equilibrium equation for the whole object, the total elements, is obtained to assemble the equation (3.13) for each element.

chapter 4

Numerical analysis of FCB in TSV structure

4.1 Bonding condition and analysis model

Numerical analysis model was developed as per the bond geometry obtained from optimized bonding condition.

4.1.1 Analysis model

Reliability of through silicon via (TSV) interconnects and interlayer bondings between the silicon layers are issues that become more complicated in 3D ICs due to the complexity of the architecture and miniaturized interconnect. Optimizing design of these devices is essential in order to avoid short fatigue life of interconnects. This manuscript addresses the impact of design parameters such as solder thickness, TSV diameter and pitch, and underfill thickness and properties on thermo-mechanical durability of direct chip attach (DCA) solder joints and TSV interconnects used in a 3D IC packages. A design was proposed where DCA is used to connect four layers of ICs and TSVs are used to connect the active layer of the dies to the second silicon layer. Solder joints, as small as 10um diameter, were used to attach silicon layers.

4.1.2 Numerical design of experimental (NDoE)

Many design parameters affect the durability of TSV interconnects and solder joints, and understanding effect of them is an important step in design step of 3D ICs. Studying all of the parameters through DoE needs a huge test matrix which requires vast amount of resources. Therefore, only four of these parameters that were considered to vary as

technology advances toward miniaturization are selected to be investigated at three levels, TSV diameter and pitch, and underfill thickness and solder thickness. In this study solder thickness was also interactively changed to keep the TSV aspect ratio fixed to five as recommended by manufacturer. These two related variables are assumed as one factor in DoE. The four variables for this study and the levels selected for these variables are listed in Table 4.1. Since the test matrix for a conventional factorial or fractional factorial DoE is very large for such a study, a Taguchi orthogonal array was selected. Taguchi arrays allow the use of smaller test matrices, but the penalty is that obtaining interaction effects is very difficult, because many of the interaction effects are confounded into main factor effects and cannot be separated. However, it will provide an accurate main effect diagram. An L9 orthogonal array is shown in Table 4.2. The first column in Table 4.2 shows the run number and the DoE variables are placed in the subsequent columns.

4.1.3 Finite element analysis

3-Dimensional parametric model of the package was built using Abaqus/CAE. Because of symmetry only a quarter model was built. Since the model contained many TSV and solder joints that needed to be meshed finely, to avoid a large number of degrees of freedom, only a strap of the package that was of interest (containing the TSV and solder joints) was modeled. Displacement boundary conditions are applied such that symmetry faces are fixed in perpendicular directions and the center of the package was fixed in all directions. An example of finite element model is shown in Fig. 4.2. Models ranged between 3000 and 6000 elements. Mesh sensitivity was conducted for one case by refining the mesh in solder joints and TSVs. Estimated durability at the point of

convergence was only 3% different from selected mesh density for this study. Therefore the mesh density deemed to be sufficient. Finite element analysis was conducted for all the runs specified in Table 4.2 and durability of solder joints and the TSV copper interconnects were calculated. The result of analysis is presented in the next section.

Parameter	1	2	3
TSV diameter (A)	10um	20um	30um
Solder thickness (B)	2um	5um	10um
TSV pitch (C)	20um	40um	60um
Underfill thickness (D)	20um	40um	50um

Table. 4.1 Parameters varied in three levels

Run	A	B	C	D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

Table. 4.2 Taguchi L9 orthogonal array

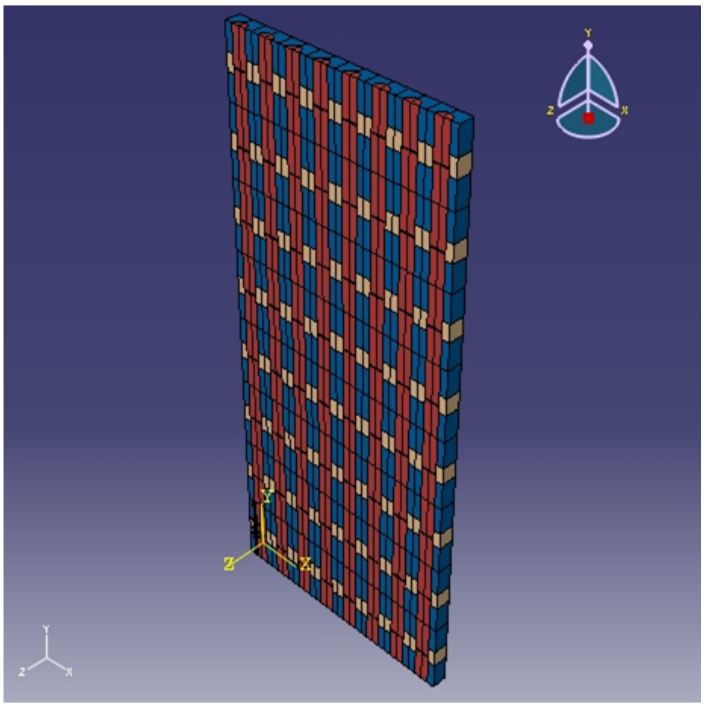


Fig. 4.1 Semi grobal model in TSV

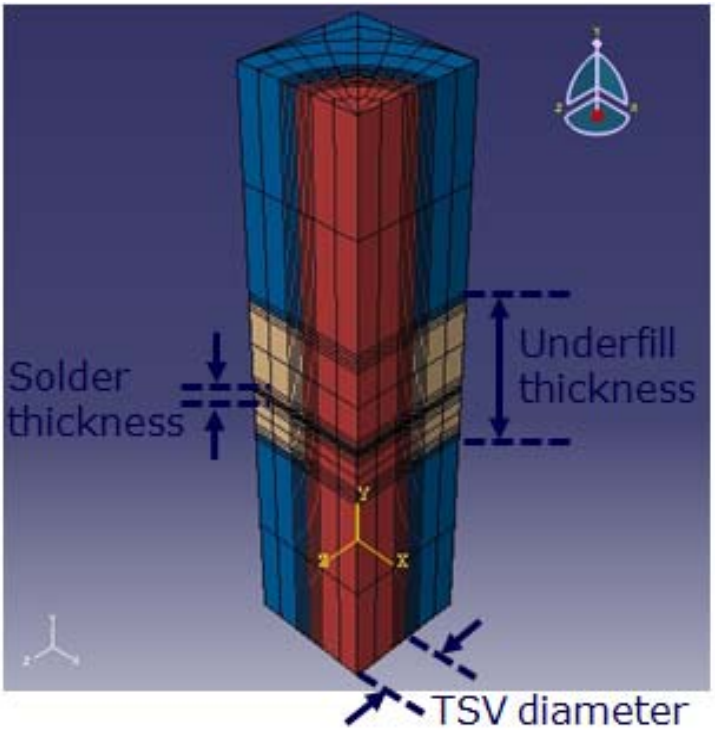


Fig. 4.2 Quarter model

4.2 Thermal-Cycling condition

Thermal Cycle Tester is used to thermally cycle products between hot and cold temperatures for accelerated durability tests. Components tested are automotive and aerospace heat exchangers. The thermal cycling is achieved by alternating convection flow from hot and cold sources. This test is conducted to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high- and low-temperature extremes. Permanent changes in electrical and/or physical characteristics can result from these mechanical stresses. This study used by JEDEC22-A104D rule. Fig. 4.3 and Table. 4.3 was shown the applied temperature condition for this study. Total time is 1190s. The dwell time and ramp time is 300s each.

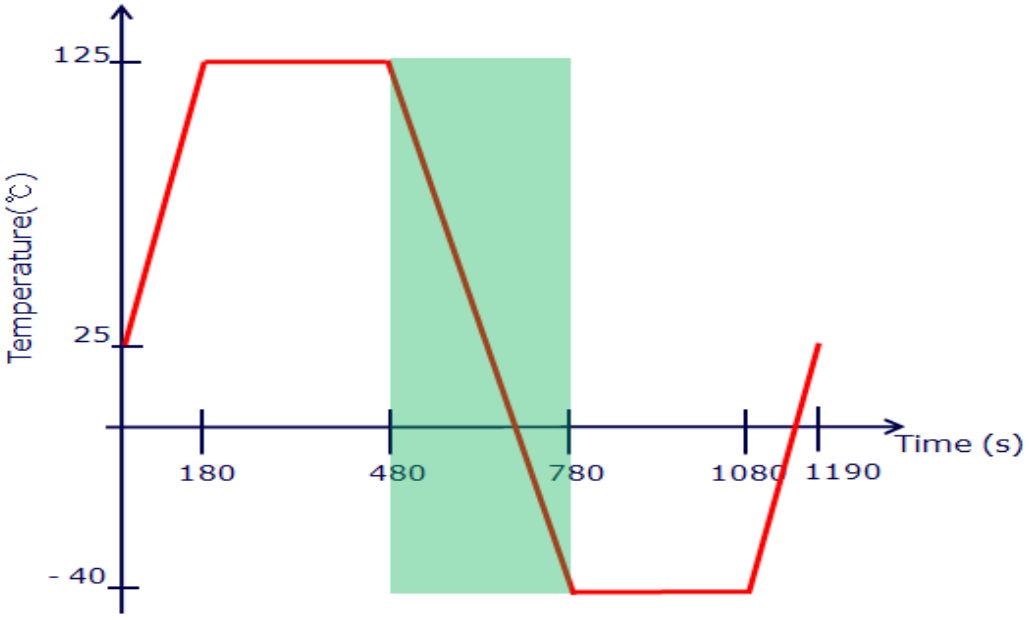


Fig. 4.3 Thermal cycling graph

	Temperature	Time
1	25	0
2	125	180
3	125	480
4	-40	780
5	-40	1080
6	25	1190

Table. 4.3 Temperature-Time amplitude

4.3 Stress distribution of 3D device

Fig. 4.4 was shown almost stress was converged solder interface and via interface. Because of CTE mismatch is very high of dissimilar materials. Also, temperature amplitude 125℃ ~ -40℃ was converged the stress. Green section is high changed temperature section. That temperature shock degree is 160℃ during 300s.

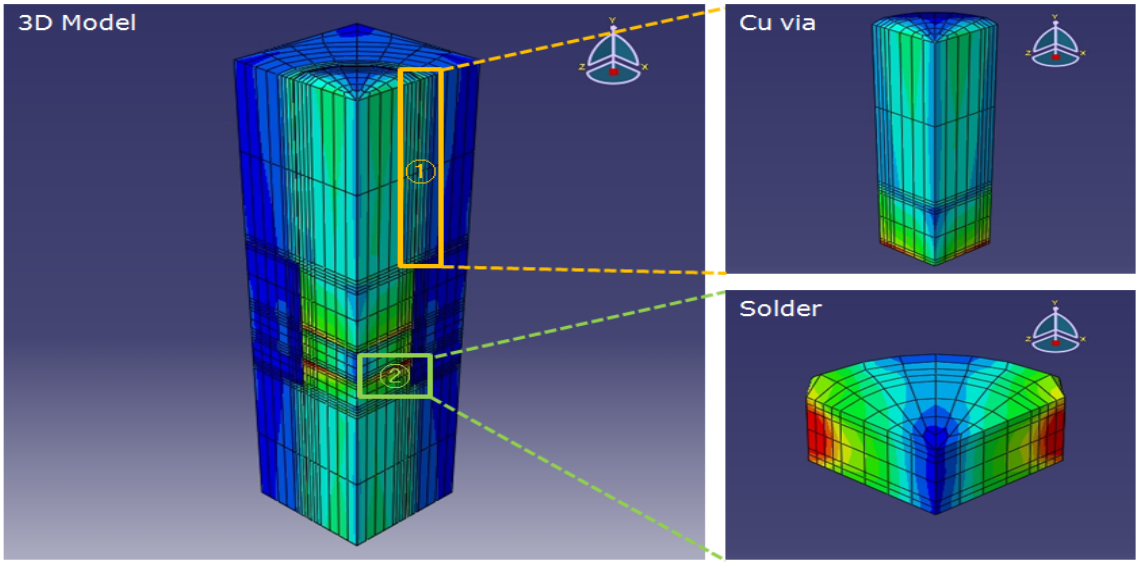
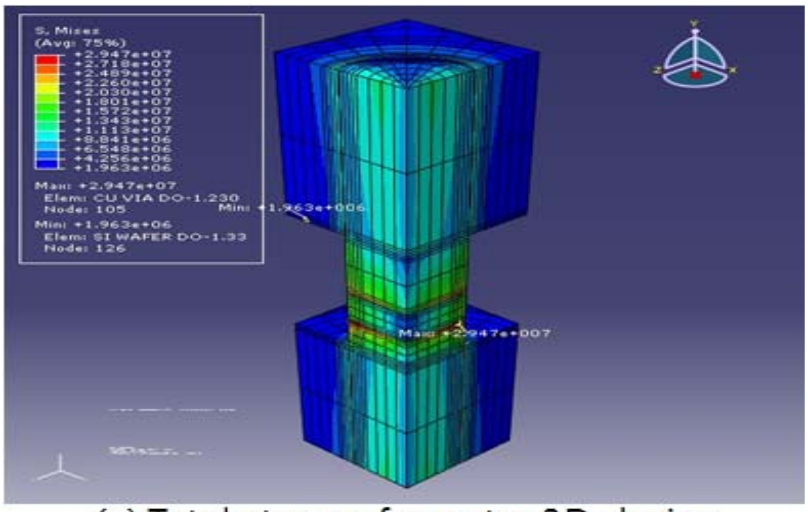
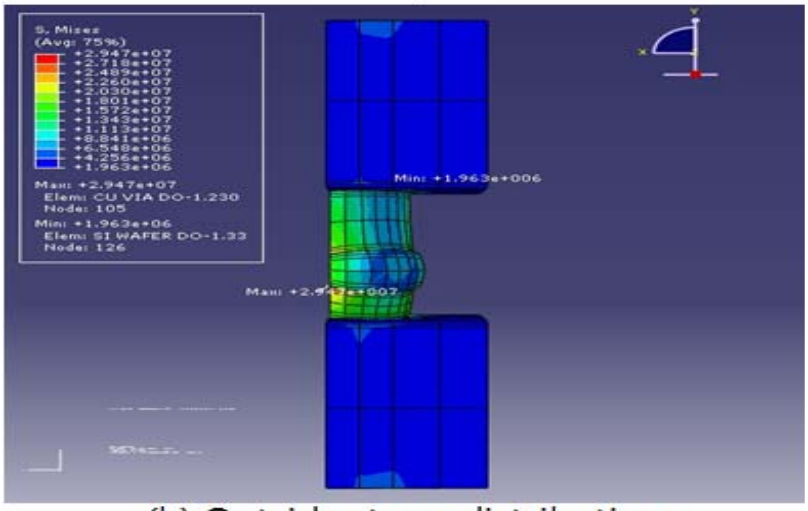


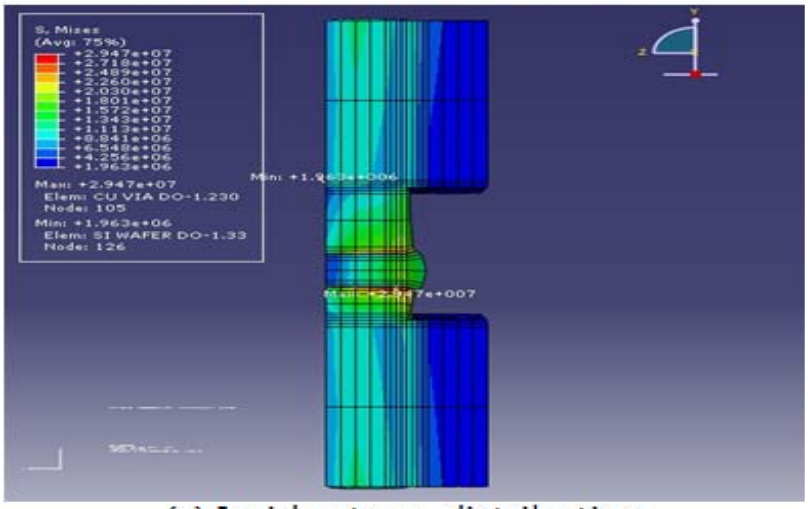
Fig. 4.4 Stress concentration of dissimilar interface



(a) Total stress of quarter 3D device



(b) Outside stress distribution



(c) Inside stress distribution

Fig. 4.5 Tendency of Stress distribution without underfill

Fig. 4.5 (a) is tendency of total stress distribution. The concentrated stress was solder interface and via interface. Fig. 4.5 (b) is outside of solder and via interface and (c) is inside of device. The Tendency of stress distribution occurred the part of material propertys (CTE, Elastic modulus) big mismatch. As follows detail explain and analysis.

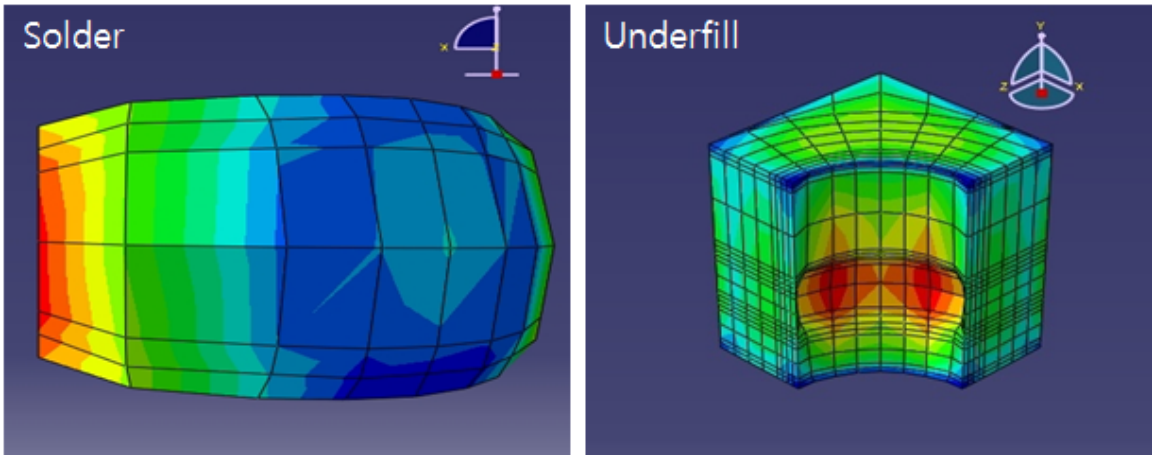


Fig. 4.6 Tendency of stress distribution solder interface

Fig. 4.6 was shown between Sn-3.5Ag solder and underfill interface stress. The stress of solder interface occurred tensile stress and underfill interface stress is compressive stress. The role of underfill prevented deformation of solder. Because of underfill character is a thermosetting property. That is decreased stress of between solder and underfill interface.

The main effect of concentrated stress of solder interface elastic modulus mismatch. Because of elastic modulus of underfill is 3000MPa and solder is 50000MPa. That is very big mismatch. Also, CTE of underfill is 30ppm/℃ and solder is 27ppm/℃. That is almost same CTE. Therefore, main effect of solder interface stress is elastic modulus mismatch of dissimilar materials.

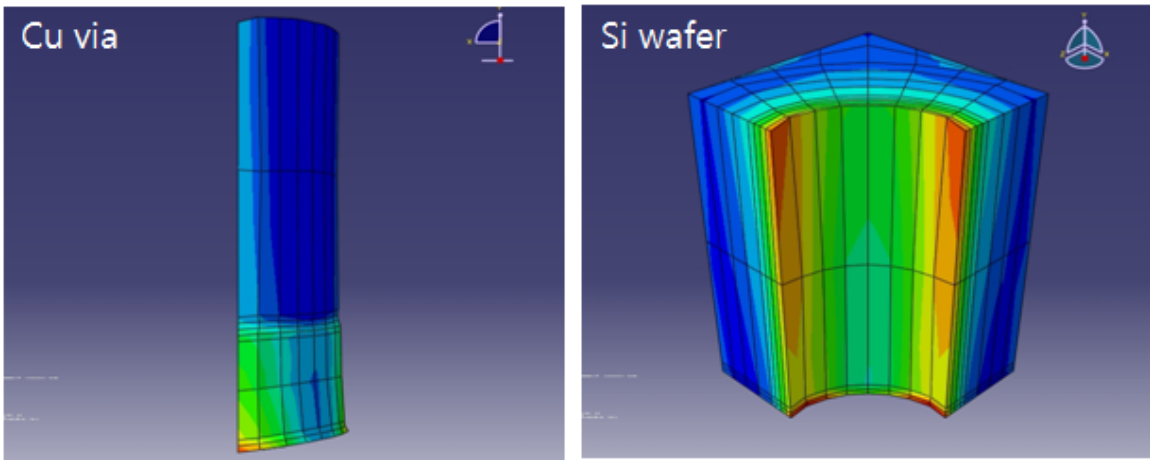


Fig. 4.7 Tendency of stress distribution via interface

Fig. 4.7 was shown between Cu via material and si wafer interface stress. The stress of via interface occurred tensile stress and si wafer interface stress is compressive stress.

The main effect of concentrated stress of via interface CTE mismatch. Because of CTE of Cu is 17ppm/℃ and si wafer is 2.8ppm/℃. The mismatch calculated 14.2ppm/℃. That is very big mismatch. Therefore, main effect of via interface stress is CTE mismatch of dissimilar materials.

4.3.1 Stress distribution of TSV diameter

Fig. 4.7 is Shown different Stress distribution in solder interface changed for TSV diameter. That selected 10, 20, 30um. Stress distribution shown 65, 35, 18MPa each other. Fig. 4.8 is Shown different Stress distribution in via interface changed for TSV diameter. That selected 10, 20, 30um. Stress distribution shown 28, 23, 18MPa each other. The more TSV diameter increased, the more decreased the stress.

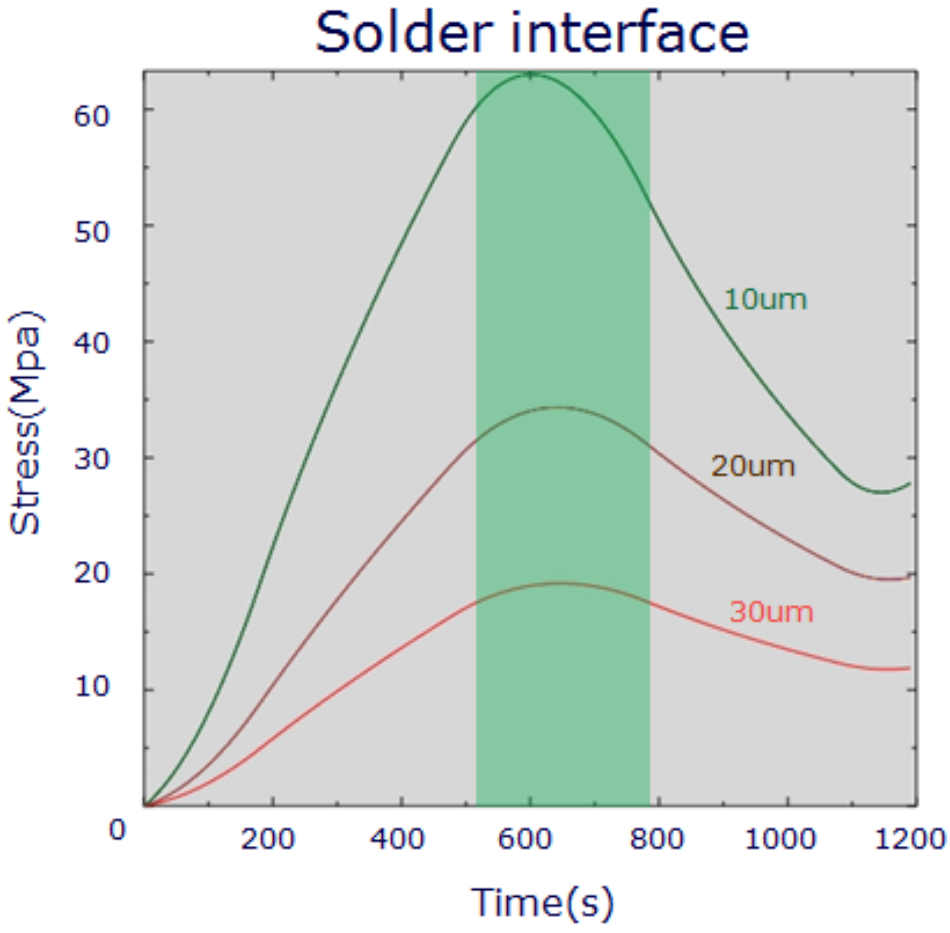


Fig. 4.7 Stress distribution of changed TSV diameter in solder interface

	10um	20um	30um
Max. Stress(Mpa)	65	35	18
Temperature(℃)	3	3	3

Table. 4.4 Stress distribution of changed TSV diameter in solder interface

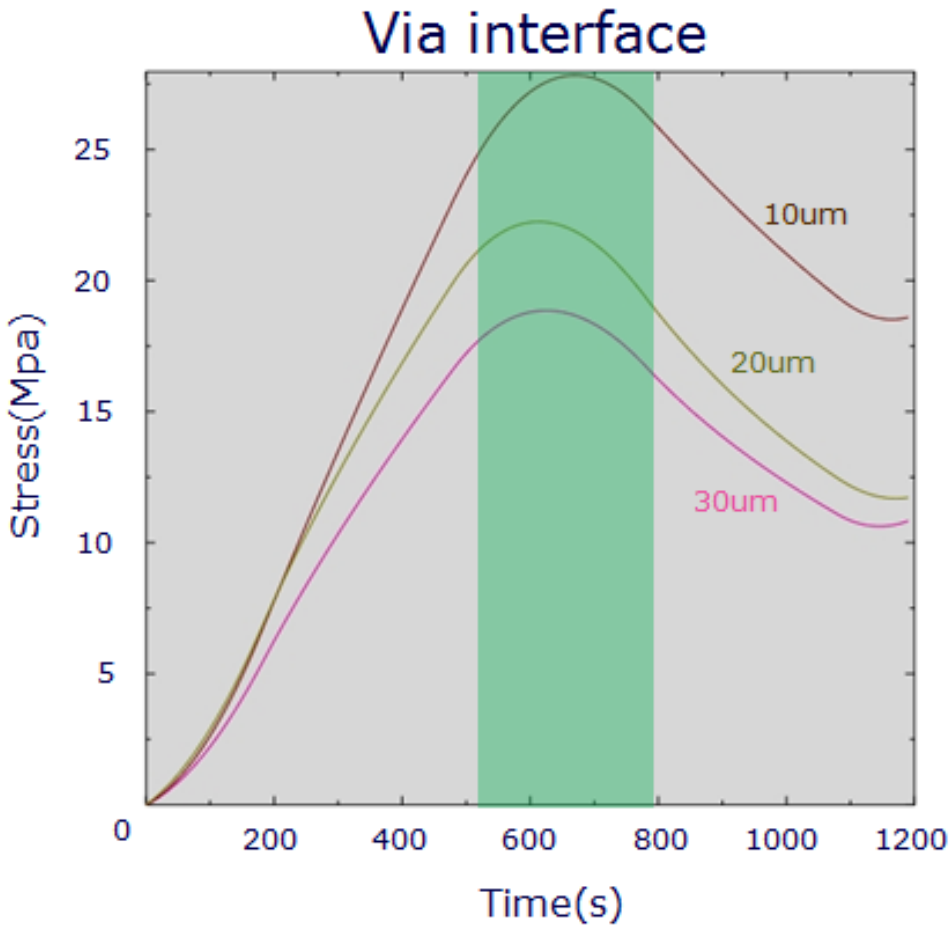


Fig. 4.8 Stress distribution of changed TSV diameter in via interface

	10um	20um	30um
Max. Stress(Mpa)	28	23	18
Temperature(℃)	3	3	3

Table. 4.5 Stress distribution of changed TSV diameter in via interface

4.3.2 Stress distribution of solder thickness

Fig. 4.9 is Shown different Stress distribution in solder interface changed for solder thickness. That selected 2, 5, 10um. Stress distribution shown 29, 46, 65MPa each other. Fig. 4.10 is Shown different Stress distribution in via interface changed for solder thickness. That selected 2, 5, 10um. Stress distribution shown 15, 16, 18MPa each other. The more solder thickness increased, the more increased the stress.

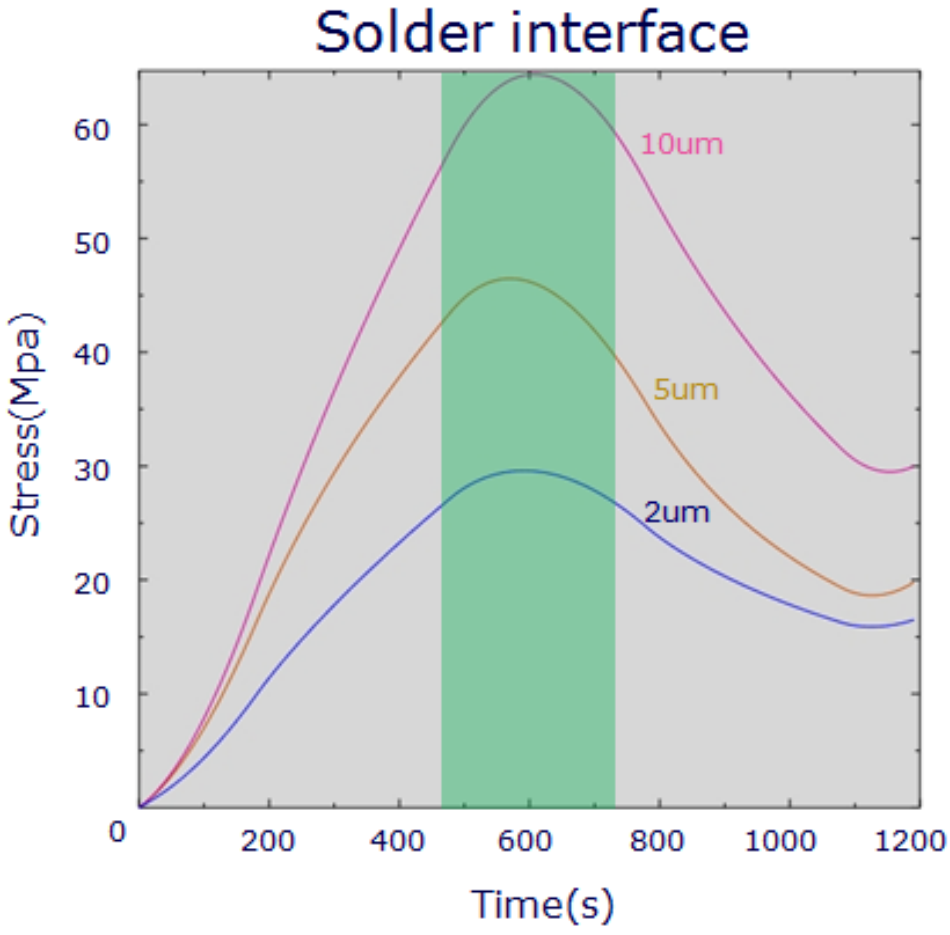


Fig. 4.9 Stress distribution of changed solder thickness in solder interface

	2um	5um	10um
Max. Stress(Mpa)	29	46	65
Temperature(℃)	3	3	3

Table. 4.6 Stress distribution of changed solder thickness in solder interface

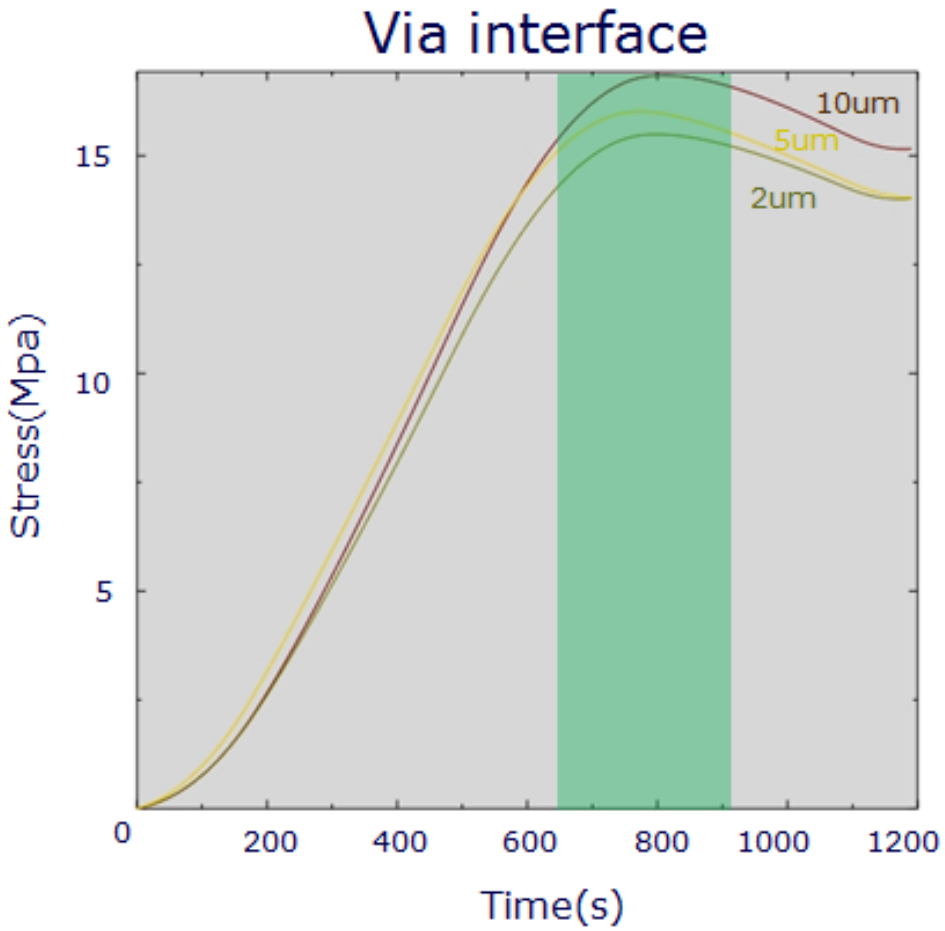


Fig. 4.10 Stress distribution of changed solder thickness in via interface

	2um	5um	10um
Max. Stress(Mpa)	15	16	18
Temperature(℃)	3~4	3~4	3~4

Table. 4.7 Stress distribution of changed solder thickness in via interface

4.3.3 Stress distribution of TSV pitch

Fig. 4.11 is Shown different Stress distribution in solder interface changed for TSV pitch. That selected 20, 40, 60um. Stress distribution shown 17, 28, 42MPa each other. Fig. 4.12 is Shown different Stress distribution in via interface changed for TSV pitch. That selected 20, 40, 60um. Stress distribution shown 6, 11, 15MPa each other. The more TSV pich increased, the more increased the stress.

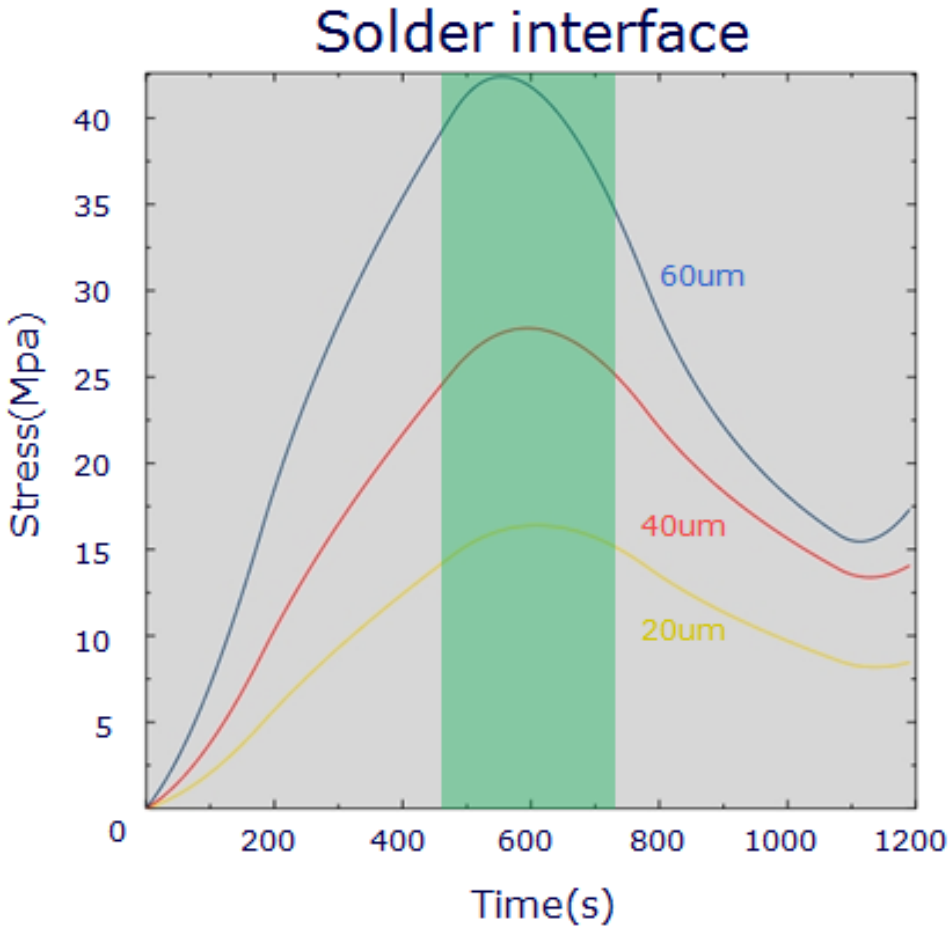


Fig. 4.11 Stress distribution of changed TSV pitch in solder interface

	20um	40um	60um
Max. Stress(Mpa)	17	28	42
Temperature(℃)	3	3	3

Table. 4.8 Stress distribution of changed TSV pitch in solder interface

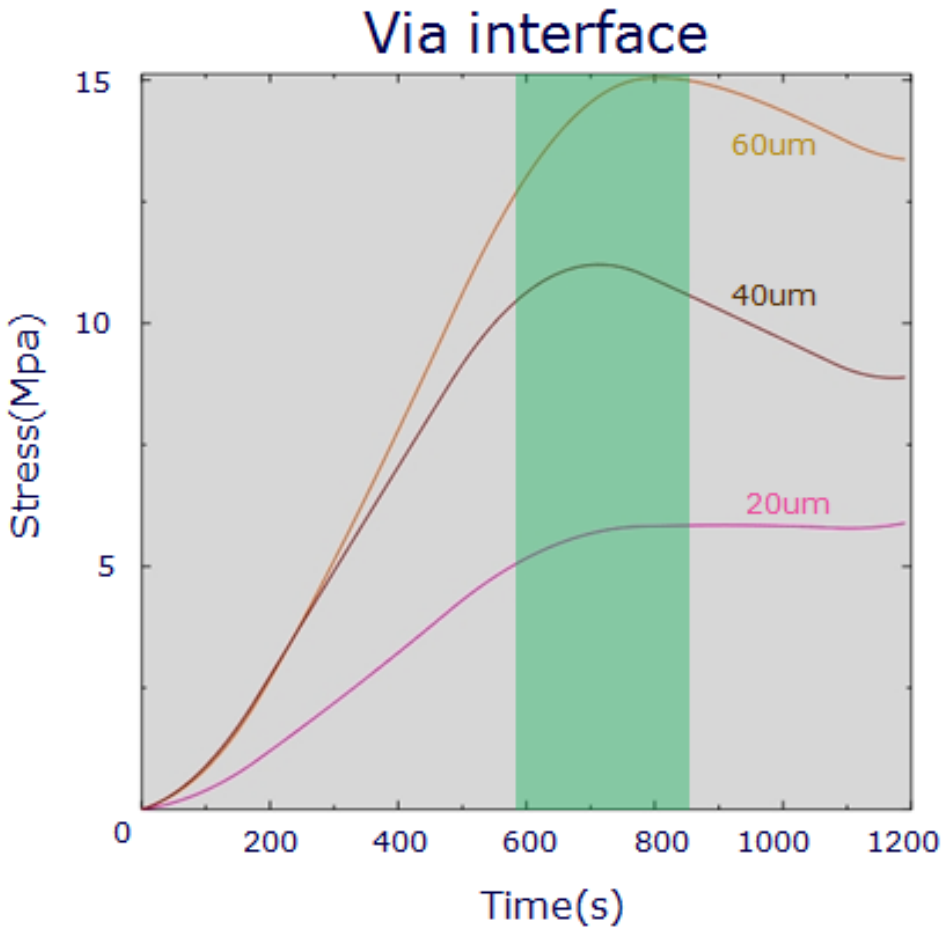


Fig. 4.12 Stress distribution of changed TSV pitch in via interface

	20um	40um	60um
Max. Stress(Mpa)	6	11	15
Temperature(℃)	3~4	3~4	3~4

Table. 4.9 Stress distribution of changed TSV pitch in via interface

4.3.4 Stress distribution of underfill thickness

Fig. 4.13 is Shown different Stress distribution in solder interface changed for underfill thickness. That selected 20, 40, 50um. Stress distribution shown 83, 59, 60MPa each other. Fig. 4.14 is Shown different Stress distribution in via interface changed for underfill thickness. That selected 20, 40, 50um. Stress distribution shown 60, 45, 36MPa each other. The more underfill tickness increased, the more decreased the stress.

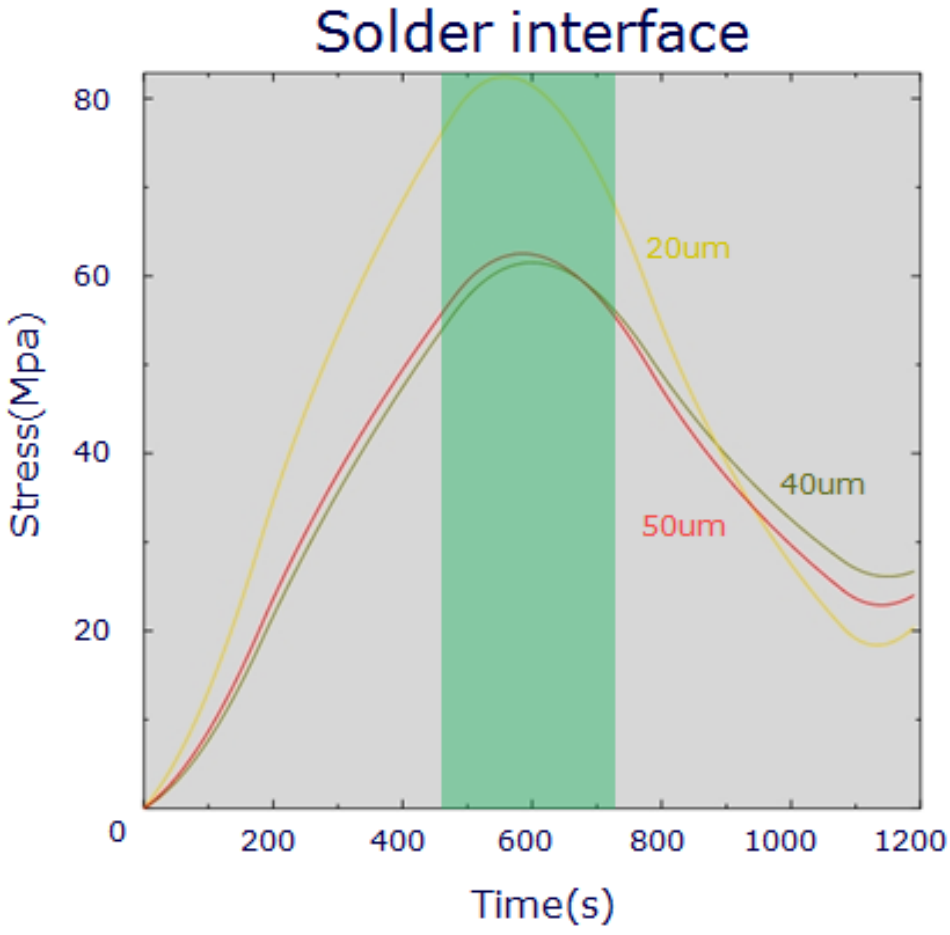


Fig. 4.13 Stress distribution of changed underfill thickness in solder interface

	20um	40um	50um
Max. Stress(Mpa)	83	59	60
Temperature(℃)	3	3	3

Table. 4.10 Stress distribution of changed underfill thickness in solder interface

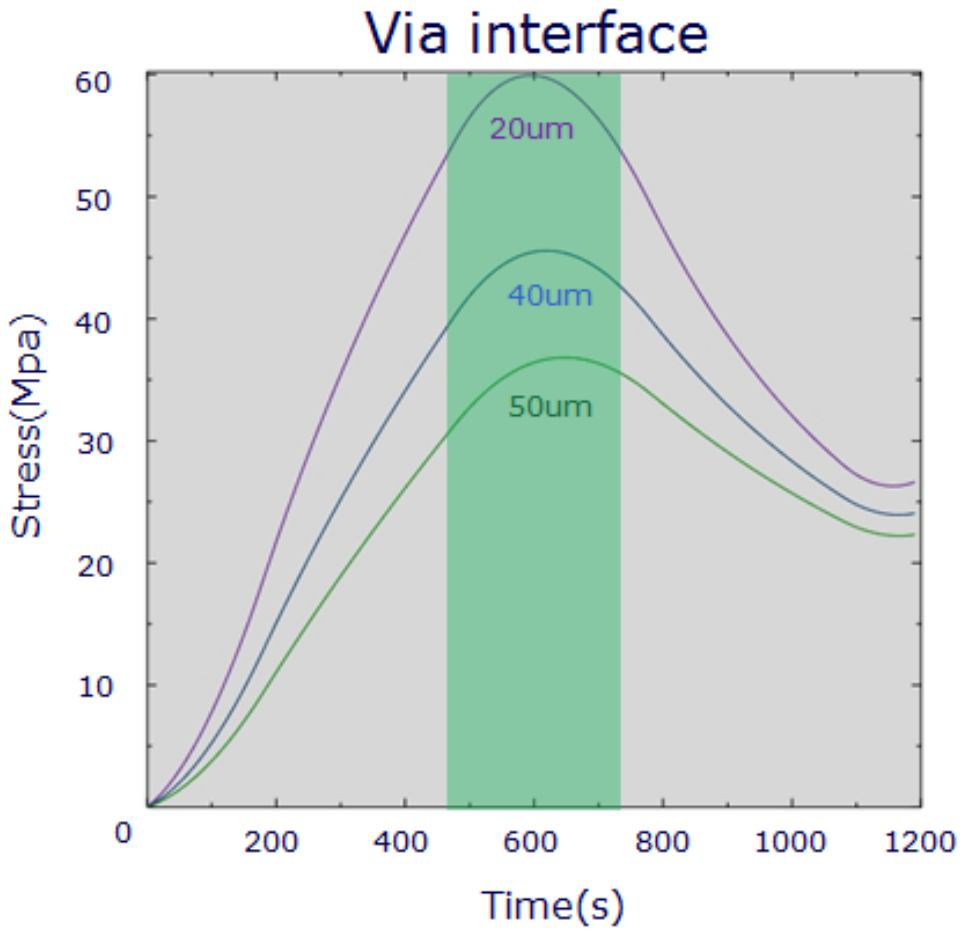


Fig. 4.14 Stress distribution of changed underfill thickness in via interface

	20um	40um	50um
Max. Stress(Mpa)	60	45	36
Temperature(℃)	3	3	3

Table. 4.11 Stress distribution of changed underfill thickness in via interface

4.4 Durability of TSV structure

Minitab software is used to analyze the result of experiment and plot main effect diagrams. The results are normalized with respect to the first run. These results are shown in Figs. 4.15 and 4.16.

As seen in Fig. 4.15 solder joint durability follows a monotonic trend for all field. As expected, as the TSV diameter increases the durability increases. Underfill usually acts as a buffer between the layers. As it becomes stiffer, it losses the capacity to deform flexibly thus inducing more deformation on solder joint resulting in increased strain energy released in solder and reducing the durability of solder joints. Increasing underfill thickness shows a monotonic increase in durability of solder joints. Increasing solder thickness increases the durability is decrease.

The same analysis was conducted for TSV interconnects. Main effect plots for TSV durability as a response parameter is shown in Fig. 4.16 In the case of TSV it can be seen from the figure that TSV diameter has a very strong effect. Reliability can be improved drastically in optimized situation where the maximum level of TSV diameter is selected. The optimized level seems to be in the selected range for all the variables except underfill thickness.

Almost parameters in solder and via interface indicated same trend. Increasing TSV diameter and underfill thickness increases the durability. Increasing solder thickness and TSV pitch decreases the durability.

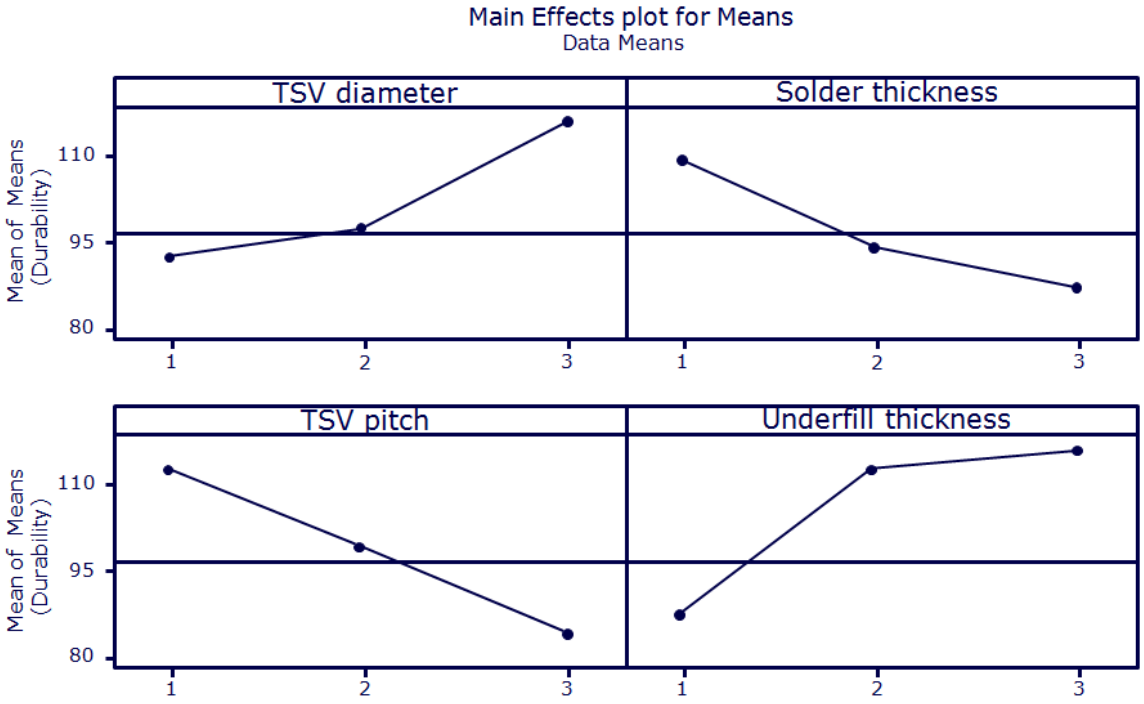


Fig. 4.15 Durability of dissimilar solder interface

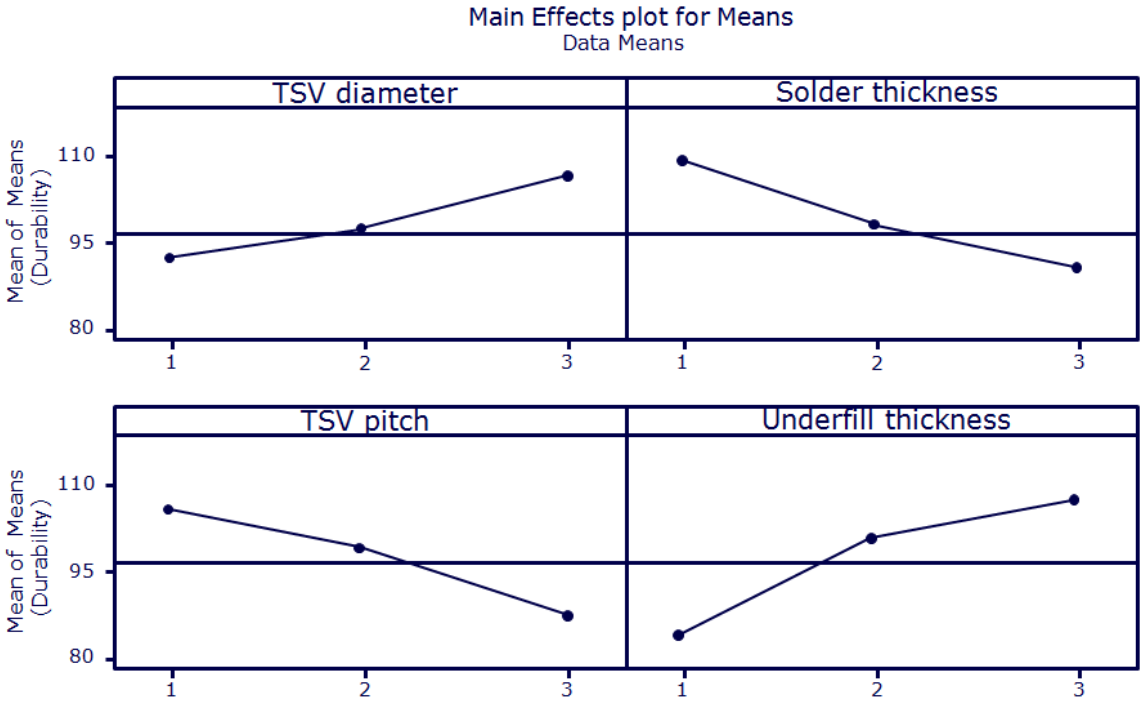


Fig. 4.16 Durability of dissimilar via interface

Chapter5
Conclusion

A numerical analysis is conducted to evaluate effect of different design parameters on thermo-mechanical durability of TSVs and solder joint interconnects in 3D ICs. A simple analytical approach is presented to find effective CTE for silicon layers with TSV copper. Statistical analysis of the result show that underfill thickness have a more significant effect on durability of solder joints than durability of TSV interconnects. It was also shown that TSV diameter is the most influential factor in determining TSV durability and that it can be modified to optimize the TSV failure location in the package. The failure site for solder joints seem to be consistent in all different cases.

1. Durability of TSV diameter
   Good state : 10um < 20um < 30um
2. Durability of solder thickness
   Good state : 2um < 5um < 10um
3. Durability of TSV pitch
   Good state : 2um < 5um < 10um
4. Durability of underfill thickness
   Good state : 2um < 5um < 10um

The most maximum stress distributed solder interface and via interface. Because of CTE mismatch of dissimilar materials. The most influential factors on durability of solder interconnect are found to be TSV underfill height. However, the most influential factor on TSV durability is found to be TSV diameter. A non-linear response was

observed for TSV pitch and diameter indicating that the optimum level is in the range selected. Location of failures was also found to depend on selected parameters and be a function of effective CTE. A simple analytical approach is presented to estimate the effective CTE for silicon layers containing TSVs. Effective CTE can be varied as one of the design parameters to achieve optimum design.

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감사의 글

항상 존경하는 마음으로 우러러 볼 수 있었고, 저에게 학문적 지식뿐만 아니라 인생의 지혜 또한 가르쳐주신 방한서 선생님께 진심으로 감사드립니다.

항상 저를 아끼시는 마음으로 조언해주고 독려해주신 방희선 교수님께 진심으로 감사드립니다.

KITECH 생활에 어려움이 없도록 신경써주시고, 인생을 설계하는 법을 가르쳐주신 이창우 박사님과 바쁘신 가운데 항상 격려와 칭찬을 아끼지 않으셨던 유세훈 박사님께 진심으로 감사드립니다.

제가 힘들 때 심적으로 많은 도움을 주고 편하게 기댈 수 있게 해준 정환이 형 감사드립니다. 그리고 같이 생활했던 용접·접합팀 식구들 즐겁고 좋은 추억들 정말 감사드립니다.

실험실 동생들의 정신적 지주 근홍이형, 항상 듬직한 준형이형, 재치있는 비조이형, 언제나 열심히인 형일이형, 유쾌한 계성이형, 항상 도움이 되어준 친구 용혁이, 동생이지만 항상 의지가 되는 두송이, 모자란 형을 잘 따라준 기상이와 정한이, 재간둥이 막내 경학이, 멀리서 고생하는 희준이 모두 감사드립니다.

그리고 못난 아들 항상 사랑으로 아껴주시고 인생의 틀을 잡아준 부모님 정말 감사드리고 사랑합니다.

저를 염려해주신 모든 분들에게 감사드리고 앞으로 더욱 성실히 생활하여 도움이 되는 사람이 될 수 있도록 항상 최선을 다하겠습니다.

박세민 드림

저작물 이용 허락서

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논문제목	한글 : TSV구조의 Via계면과 Cu-Sn 합금-Cu 플립칩 접합부의 열에 의한 역학적 특성 평가 영어 : Thermo-mechanical analysis of Cu-Sn alloy-Cu flipchip bonding and via interface in TSV structure				

본인이 저작한 위의 저작물에 대하여 다음과 같은 조건아래 조선대학교가 저작물을 이용할 수 있도록 허락하고 동의합니다.

- 다 음 -

1. 저작물의 DB구축 및 인터넷을 포함한 정보통신망에의 공개를 위한 저작물의 복제, 기억장치에의 저장, 전송 등을 허락함
2. 위의 목적을 위하여 필요한 범위 내에서의 편집·형식상의 변경을 허락함. 다만, 저작물의 내용변경은 금지함.
3. 배포·전송된 저작물의 영리적 목적을 위한 복제, 저장, 전송 등은 금지함.
4. 저작물에 대한 이용기간은 5년으로 하고, 기간종료 3개월 이내에 별도의 의사 표시가 없을 경우에는 저작물의 이용기간을 계속 연장함.
5. 해당 저작물의 저작권을 타인에게 양도하거나 또는 출판을 허락을 하였을 경우에는 1개월 이내에 대학에 이를 통보함.
6. 조선대학교는 저작물의 이용허락 이후 해당 저작물로 인하여 발생하는 타인에 의한 권리 침해에 대하여 일체의 법적 책임을 지지 않음
7. 소속대학의 협정기관에 저작물의 제공 및 인터넷 등 정보통신망을 이용한 저작물의 전송·출력을 허락함.

동의여부 : 동의(O) 반대( )

2011 년 8 월

저작자: 박 세 민 (서명 또는 인)

조선대학교 총장 귀하