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碩士學位論文

Hearing Aids Specialized CMOS Analog Integrated Circuit Design

朝 鮮 大 學 校 大 學 院

制御計測工學科

陳 凌 峰

보청기 전용 CMOS 아날로그 IC 칩 설계

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指導敎授　張　淳　晳

이 논문을 工學碩士學位申請 論文으로 提出함.

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2005 年 5 月 日

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V_{DSAT}	Saturation Voltage
R_D	Drain Source Resistor
V_{DD}	Positive Supply Voltage
V_{SS}	Negative Supply Voltage
CMRR	Common Mode Rejection Ratio
C_M	Miller Capacitor
G_m	Circuit Transconductanc
g_m	Device Transconductanc
V_T	Threshold Voltage
V_{T0}	Threshold Voltage at Vsb = 0V
W	Channel Width
L	Channel Length
V_{DS}	Drain-Source Voltage
V_c	Common Mode Input Voltage
V_d	Differentia Mode Input Voltage
χ	the rate of change of the threshold voltage with body bias voltage
λ	Channel Length Modulation Parameter.
C_{ox}	capacitance per unit area of the gate oxide (F/cm^2) $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ ε_0 is permittivity of free space, ε_{ox} is permittivity of SiO_2; t_{ox} is thickness of the SiO_2
u_o	surface mobility of the channel for the n-channel or p-channel device ($cm^2/C-s$))

Abstract

Hearing Aids Specialized CMOS Analog Integrated Circuit Design

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The research is based on hearing aids specialized CMOS analog integrated chip (IC) design. The hearing aids IC design faces the challenges from the constraints of its special applications on In-The-Ear (ITE) hearing aids. Firstly, The chip works on a single supply voltage of 1.3V. With the single supply, or we may say a single battery, the hearing aid can be made small enough to be completely put into the ear canal. Secondly, a low power dissipation is required. It makes the battery lasts longer, gets less thermal noise, etc.

The efforts on solutions to the two issues can be found on different areas. In this thesis, I tried short channel processes in order to get a low supply as well as a low power consumption.

I tried two different short channel processes, ANAM-0.18um and Samsung-0.18um. Two design methods, a optimization design and a transistor scale ratio design were also introduced. These methods achieve a high accuracy and efficiency on the prediction of deep-submicron device circuit parameters.

Keywords: Hearing Aid, CMOS analog design, low voltage op-amp, single-supply op-amp.

I. Preface

The hearing aid chips on market recently are mainly of two types; analog and digital hearing aid (HA) integrated chips. The digital HA ICs have many merits compared with the analog ones such as more functions and flexibilities and are more favored. There is a tendency of building complex algorithms into digital processors in order to get a higher performance. It is the reason why digital HA ICs are getting so popular today. However, the analog circuits can be found as essential blocks in any digital hearing aid integrated system. Since the A/D converters, D/A converters work as interfaced between real analog world and digital processors. The regulators provide a steady supply. And may other analog circuits are playing rather important role in integrated systems. Therefore, the research on analog circuits is of a great importance and worthwhile.

The present research purpose is to design hearing aid specialized analog and analog part of ICs. It starts with the design of some basic analog building blocks such as operational amplifiers, regulators and output buffers, etc. In order to get practical results, I did both front-end and back-end designs to be apply for MPW (Multi-Project Wafer) Desig in IDEC. I hope the research may contribute to both hearing aids design and the low voltage CMOS IC design as well.

Section II shows general idea of design flow of IC both on semi-custom and full custom. Some industrial design tools are also introduced.

Operational Amplifiers (Op-amp) are most versatile and important building blocks of functional analog circuits. Section III of the thesis states building blocks of op-amps. Differential pairs, common-source gain stages, output buffers are analyzed in detail.

In section IV, a two-stage Miller compensation op-amp is designed with the method of hand calculation combined with Hspice optimization. The comparison between the optimized and the non-optimized op-amps shows how it works.

Section VI deals with the design of hearing aids application op-amps. A single-supply, low voltage op-amp is designed.

All the spice netlists are listed in appendix.

II. Introduction on Integrated Circuit Design

The Very Large Scale Integration (VLSI) technology is developing rapidly in the last decade. It becomes possible to integrate millions of transistors on a single die. The integrated circuits were used to be made into subsystem components while now people integrate complete systems with both analog and digital functions on one chip. The Complementary Metal-Oxide Semiconductor (CMOS) technology has been the main implementation on analog digital mixed-signal because of its density as well as its power saving on digital design and a good mix of components for analog design. [1]

Generally speaking, there are three different integrated circuit design flows, semi-custom design, full-custom design and mixed-mode design. In semi-custom design, an integrated circuit is designed either by using existing blocks of design elements of is made on an existing array of gates which are just connected together to form a new circuit. Usually, semi-custom design is often used to implement complex digital systems. Most popular implementations are standard cells and FPGA design. In semi-custom design, the designers do not need to bother themselves with the transistors, resistors and capacitors. The design is based on pre-made building blocks such as gate circuits, simple function circuits, etc. Compared with semi-custom, full-custom design is much more complex. After getting a transistor level design schematic, the designer describe the circuit with spice or schematic design tools to get a circuit net list. Simulation, layout and verification are essential. Mixed-mode design includes both standard cells and full-custom design. It is greatly helpful for reducing the developing period of analog-digital mixed system. The designer can use the standard cells library in digital part and design their analog part as well.

However, the automatic layout result should be adjusted when digital and analog parts are put together.

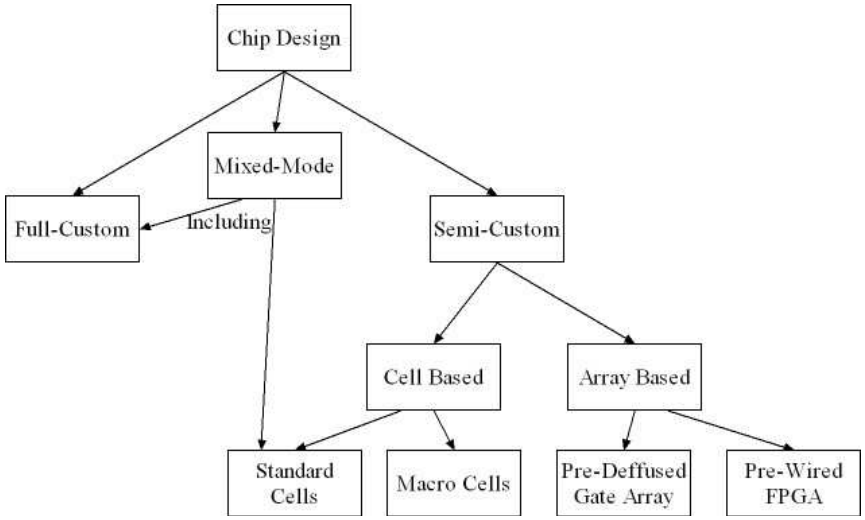


Fig. 2-1 IC Implementation Methodology

A. Semi-Custom Design Flow

In semi-custom design, an integrated circuit is designed either by using existing blocks of design elements or is made on an existing array of gates which are just connected together to form a new circuit. It includes cell based-design and array-based design. Standard cell design is one of most widely used cell-based design, which develops predefined implementations of the basic gates with standard form-factor. It uses regular layout and can automate the mapping process.

Step	Name	Input file	Output file	Tools
1	Chip Specification	--		--
2	System Level Define			--
3	Algorithm Selection	--	--	--

4	Algorithm Verification	--	--	C /SystemC /Matalab
5	RTL Description (VHD, Verilog)	--	*.vhd/*.v	Coding
6	Function Verification	*.vhd/*.v	Waveform	ModelSim
7	Synthesis	RTL HDL, Cell libraries, Constraints	Gate-Level Netlist	Design Complier
8	Static Timing Analysis	Constraints	Report	Prime Time
9	Formal Verification	--	--	
10	DFT	--	--	DFT Compiler
11	Gate Level Simulation (Pre-layout Simulation)	Gate-Level Netlist, Test Bench, Constraints	Waveform	ModelSim
12	Place & Route	Gate-Level Netlist, Layout Cell Library	GDSII	Apollo
13	DRC & LVS	GDSII, Design Rules File, Layout Database	Error Report, GDSII	Calibre, IC_Station

Table 2-1. Semi-Custom Design Flow.

Chip Specification. Firstly, we get an idea on design and specify our requirements.

System Level Definition. After chip specification, we need to define the operation conditions such as working temperature, voltage, power, area, chip function, input/output condition, etc. Actually it is quite important to our design.

Algorithm Selection. With the specifications, we select the proper algorithms for the design.

Algorithm Verification. On this step, we use high level programming language to verify the algorithms we selected. The verifications are both done on function and efficiency.

HDL description. We can describe our design with VHDL or Verilog HDL. The coding style should be based on the idea of hardware and synthesis.

Function Verification. The EDA tools, such as XL-Verilog, Modelsim, VCS, are used here to simulate the HDL coding of our design. To stimulate the circuit, we also write a stimulus file, which is named as a test bench, to provide circuit with input signals.

Synthesis. Synthesis is the transformation of an idea into a manufacturable device to carry out an intended function. If the function verification is successful, we start synthesis. One of the most popular synthesis tools is Design Compiler, a wonderful product of Synopsis. In this step, the VHDL/Verilog HDL coding is translated, optimized and mapped. The output file, a gate level netlist, is an input file of the next Place & Route tools. The device libraries are introduced into the design on this step. That is, our design is related to the vender through the synthesis.

Static Timing Analysis (STA). STA can determine if a circuit meets timing constraints without dynamic simulation. It works like this: the design is broken down into sets of timing paths and the design tool calculates and checks the time delay of each path to see if timing constraints have been met. We use Prime Time, another successful tool of Synopsys to perform STA.

(Note, The timing constraints are input and output delay of ports or devices, which are defined in a constraints file or item by item on synthesis.)

Formal Verification. It is an optional flow.

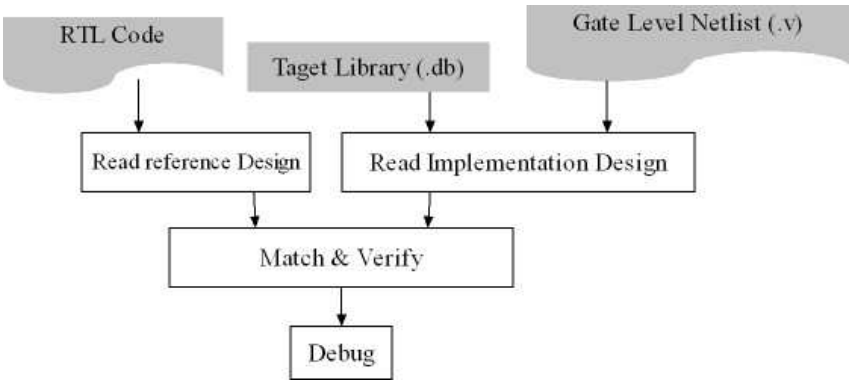


Fig. 2-2 Formal Verification

DFT. Design for Test is an optional flow.

Gate-Level Simulation (Pre-layout Simulation). The synthesis translates, optimizes and maps our descriptions of the design into real gate level circuit according to the vender libraries. Our initial design is modified slightly here and there. So we have to simulate the gate-level netlist again to confirm the function of the circuit.

Place & Route. In Semi-Custom design, people use auto-Place & Route tools to place and route there designing. A layout cell library which relates to the synthesis cell library is a component to P&R tools. It provides the detail physical property information on the cells used in circuit while the synthesis cell library provides electrical and timing properties.

DRC, LVS & PRC. DRC is design rule check. The input files of DRC tools are GDSII files generated by P&R and design rule file provided by the venders. With these files, the DRC tools check the layout results to ensure that the entire layout meets the process design rule. LVS is Layout Versus Schematic. It compares layout with the schematic and gets the report from that. Also, the netlist can be extracted from this step.

Post-layout Simulation.

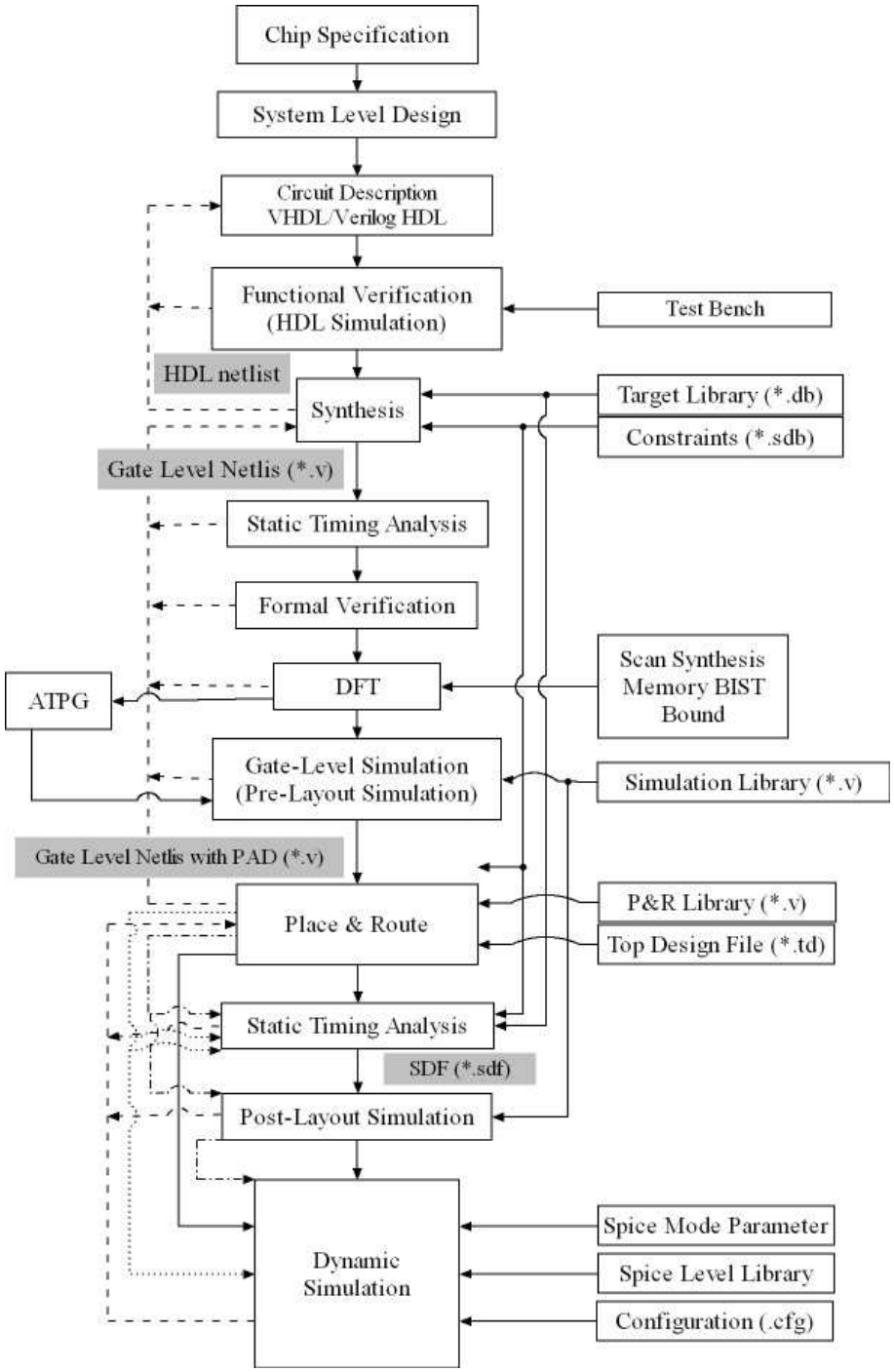


Fig. 2-3 Diagram of Standard Cell Based Integrated Circuit Design Flow

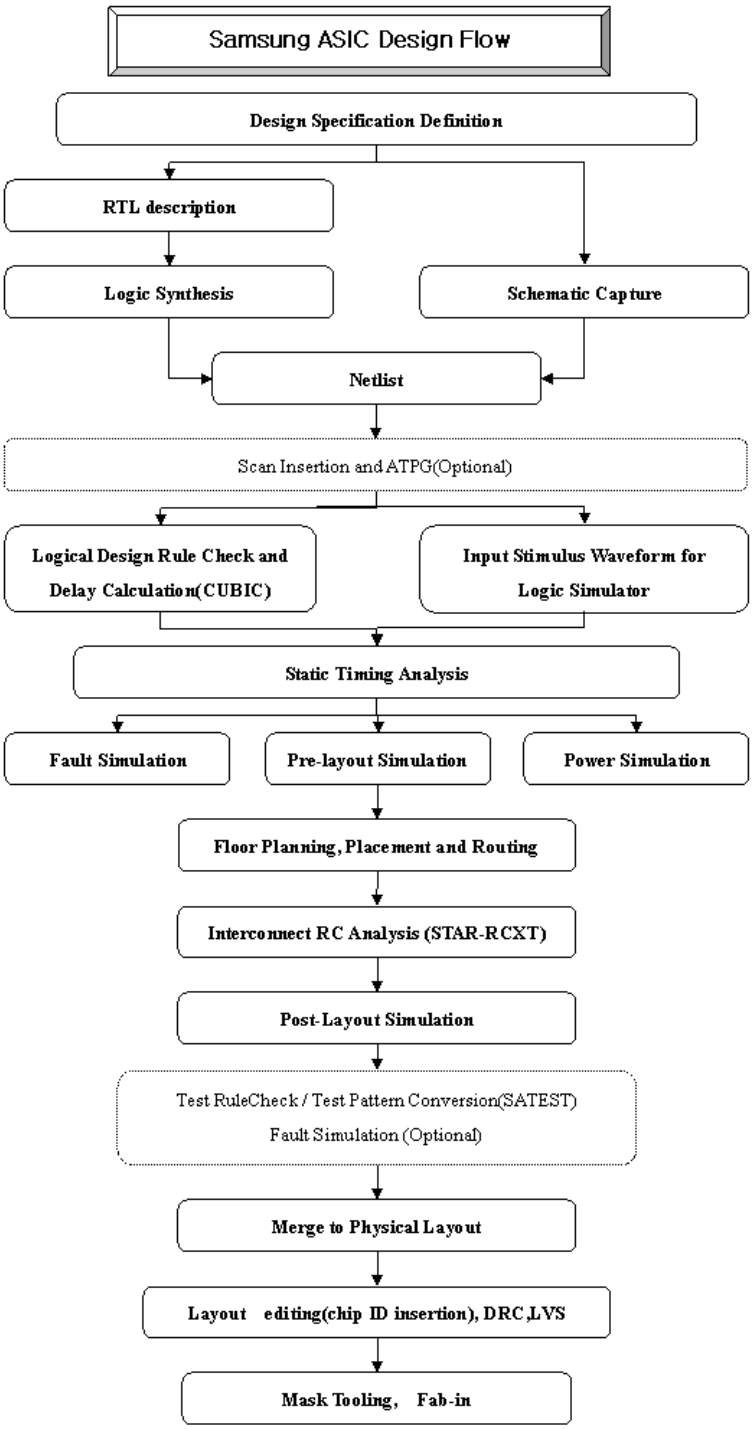


Fig. 2-4 Diagram of Samsung ASIC Design Flow

B. Full-Custom Design Flow

In Full-Custom design, we design transistor level schematic, simulation and layout. Because we complete the design completely for the special application, we can get exactly what we want. However, it is complex, time consuming and takes a high design cost.

1. *Chip Specification.*
2. *Transistor Level Design.* It defines the detail parameters such as capacitor values, resistor values, transistor widths and lengths, etc. The Hspice provides some optimal design tools, but it still depends on the accurate results of the hand calculation.
3. *Circuit Simulation.*
4. *Layout Design.*
5. *Layout Verification (DRC/LVS)*
6. *Parasitic RC Extraction.*
7. *Post-Layout Simulation.*

Step	Name	Input file	Output file	Tools
1	Chip Specification	--	--	--
2	Transistor Level Design	--	--	--
3	Circuit Simulation	--	--	Hspice, Awaves
4	Layout	--	GDSII	Virtuoso
5	Layout Verification DRC & LVS	GDSII, Design Rules File, Layout Database	Error Report, GDSII	Calibre, IC_Station
6	Layout Parasitic Extract	GDSII	Error Report,	Hercules &

	(LPE)		GDSII, Spice	Star-RCXT
7	Static Timing Analysis	GDSII	Error Report	Prime Time
8	Post-layout Simulation	Spice	Waveform	Hspice, Awaves
9	Dynamic Simulation	--	--	--

Table 2-2 Full-Custom Design Flow

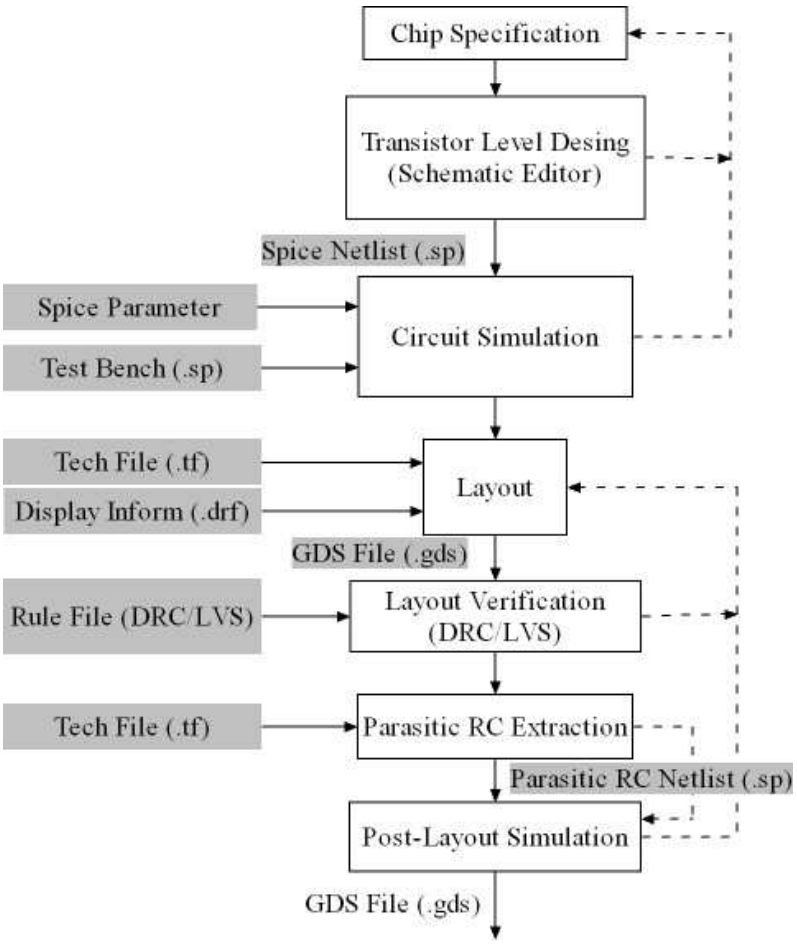


Fig. 2-5 Diagram of Full-Custom Integrated Circuit Design Flow

C. Mixed-Mode Design Flow

Mixed-mode includes standard cells library design as well as the full-custom design. It is the most popular approach we take to implement a complex system which has digital processors and the analog supporting circuits.

III. Operational Amplifier Building Blocks

Operational amplifiers (op-amps) are most versatile and important building blocks of functional analog circuit. They are used quite often on analog filters, power-amplifiers, analog-to-digital (A/D) converters digital-to-analog (D/A) converters, regulators, etc. Therefore, qualified operational amplifiers are of great importance in both analog and analog digital mixed-mode integrated circuit design.

Generally speaking, an op-amp consists of following components, a differential transconductance stage, a high gain stage, an output buffer, a compensation circuitry and a bias circuitry.

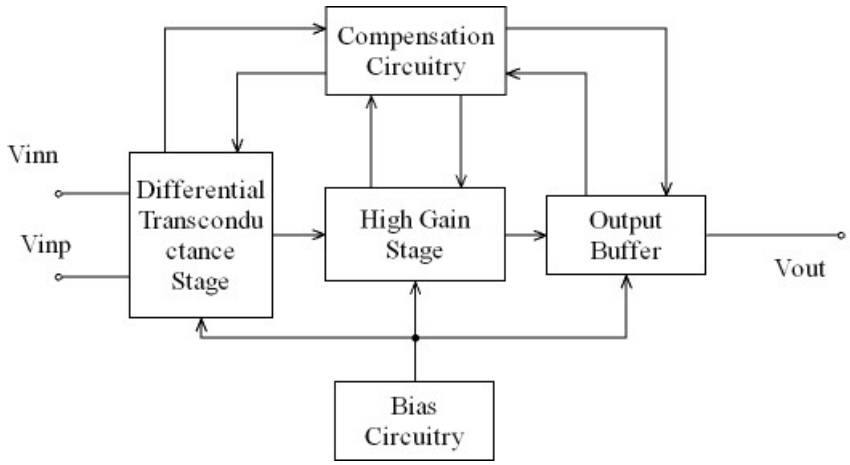


Fig. 3-1 Block Diagram of a General Two-Stage Op-amp

The Differential pairs are the most popular structure used as an input stage. It provides a very large input impedance and part of the gain as well. The high gain stage gets the majority of the gain. And the output buffer keeps the output impedance at a low level. To get an acceptable phase margin, we add a frequency compensation network regarding the load. The most common

frequency compensation technique is Miller compensation. Later section shows the technique in detail. In this section, analysis is given to each block circuit.

Assume that the channel length is not very short and the square law still works. So the calculation is based on the square law.

[Square law is

A. Differential Pairs

N-Channel Differential Pair Analysis

The differential input stage module shown on Fig. 3-2 is a N-channel differential pair with resistor load, R_D. V_{i1} and V_{i2} are two inputs while V_{o1} and V_{o2} are two outputs. So we can define common mode signal and differential mode signal through these signals.

Common mode signals:

$$V_{ic} = \frac{V_{i1} + V_{i2}}{2} \qquad (3\text{-}1)$$

$$V_{oc} = \frac{V_{o1} + V_{o2}}{2} \qquad (3\text{-}2)$$

Where V_{ic} is the input common mode signal; V_{oc} is the output common mode signal.

Differential mode signals:

$$V_{id} = V_{i1} - V_{i2} \qquad (3\text{-}3)$$

$$V_{od} = V_{o1} - V_{o2} \qquad (3\text{-}4)$$

Where V_{id} is the input common mode signal; V_{od} is the output common mode signal.

With Equation 3-1 to 3-4 we can get

$$V_{i1} = V_{ic} + \frac{V_{id}}{2} \qquad (3\text{-}5)$$

$$V_{i2} = V_{ic} - \frac{V_{id}}{2} \quad (3\text{-}6)$$

$$V_{o1} = V_{oc} + \frac{V_{od}}{2} \quad (3\text{-}7)$$

$$V_{o2} = V_{oc} - \frac{V_{od}}{2} \quad (3\text{-}8)$$

1 Large-signal model analysis (DC)

The first step is to analyze the large signal performance.

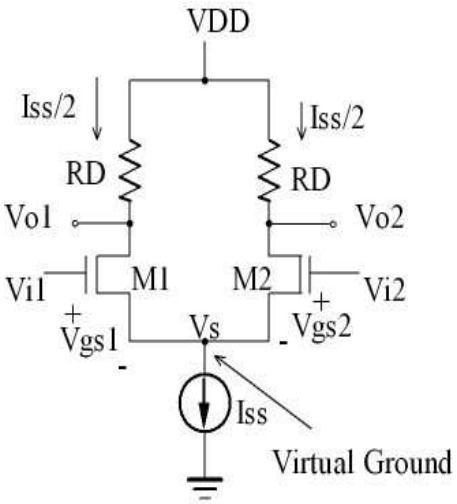


Fig. 3-2 Resistor Load N-Channel Differential Pair

Because there is no additional current through the equivalent current source, Iss the point Vs is a virtual grand.

Assume that the two inputs are not the same.

a. If the V_{i2} is so small that it makes the transistor M2 cutoff. That is,

$$V_{i2} < V_{TN} + V_{DSAT} \quad (3\text{-}9)$$

and $$V_{i1} > V_{TN} + V_{DSAT} \quad (3\text{-}10)$$

Where the V_{TN} is the threshold voltage of the N transistor, M1 and M2; V_{DSAT} is the saturation voltage of the transistors M1 and M2.

The M2 cutoffs and all the current from the current source flows into the M1. In this case, the output is:

$$V_{od} = V_{o1} - V_{o2} \quad (3\text{-}11)$$

Where

$$V_{o1} = V_{DD} - I_{SS} \cdot R_D \quad (3\text{-}12)$$

$$V_{o2} = V_{DD} \quad (3\text{-}13)$$

$$V_{od} = V_{o1} - V_{o2} = V_{DD} - I_{SS} \cdot R_D - V_{DD} = - I_{SS} \cdot R_D \quad (3\text{-}14)$$

b. If the V_{i1} is so small that it makes the transistor M1 cutoff.

$$V_{i2} > V_{TN} + V_{DSAT} \tag{3-15a}$$

$$V_{i1} < V_{TN} + V_{DSAT} \tag{3-15b}$$

The transistor M1 cutoffs and all the current from the current source flows into the transistor M2. In this case, the output is:

$$V_{od} = V_{o1} - V_{o2} \tag{3-16}$$

Where

$$V_{o1} = V_{DD} \tag{3-17}$$

$$V_{o2} = V_{DD} - I_{SS} \bullet R_D \tag{3-18}$$

$$V_{od} = V_{o1} - V_{o2} = V_{DD} - V_{DD} + I_{SS} \bullet R_D = I_{SS} \bullet R_D \tag{3-19}$$

c. If both of the transistor work in saturation area, we have,

$$V_{i1} - V_{gs1} + V_{gs2} - V_{i2} = 0 \tag{3-20}$$

$$I_{DS1} + I_{DS2} = I_{SS} \tag{3-21}$$

$$V_{gs1} = V_{T1} + \sqrt{\frac{2 \bullet I_{DS1}}{k' \bullet \frac{W_1}{L_1}}} \tag{3-22}$$

$$g_m = \sqrt{2k' \frac{W}{L} I_{DS}}, \quad (k' = u \bullet C_{ox}) \tag{3-23}$$

$$\Delta V_{id} \approx \frac{I_{SS} \cdot R_D}{SLOPE} = \frac{I_{SS} \cdot R_D}{g_m \cdot R_D} = \sqrt{\frac{I_{SS}}{k' \cdot \frac{W}{L}}} \tag{3-24}$$

Where V_{gs1}, V_{gs2} are the Gate Source voltage of M1 and M2; I_{DS} is the Drain Source current; V_{T1} is the threshold voltage of the transistor M1; I_{SS} is the current of the current source. The SLOPE in Equation 3-24 is the slope of the Vin vs Vout curve shown in Fig 3.3(a). ΔV_{id} is the difference of $V_{i1} - V_{i2}$.

Note, when the differential input signal is zero, the differential output signal should equal to zero. Otherwise we shall add a offset voltage. Fig. 3-3 (a)

shows the output versus input curve. When the input differential signal is larger than the ΔVid, which is around 2 or 3 times of saturation voltage V_{DSAT}, the circuit gets its positive/negative maximum value, $I_{ss}R_D/-I_{ss}R_D$. Fig. 3-3 (b) shows a simulation result of DC voltage transfer characteristic of a single-supply N-channel differential pair.

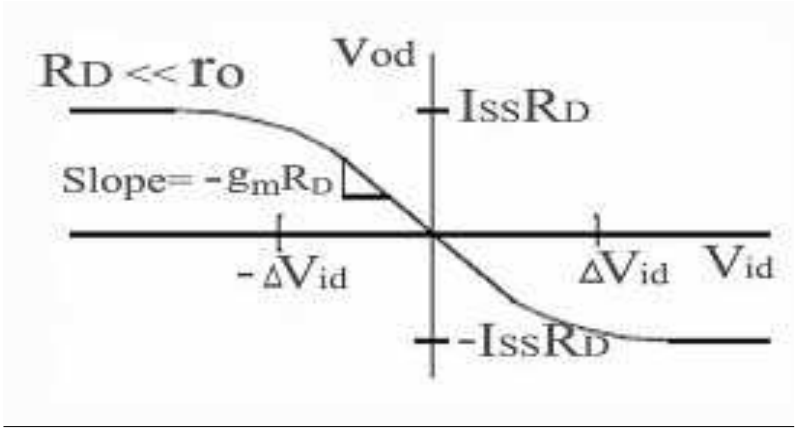


Fig 3-3 (a) Differential Mode Output VS Input Curve

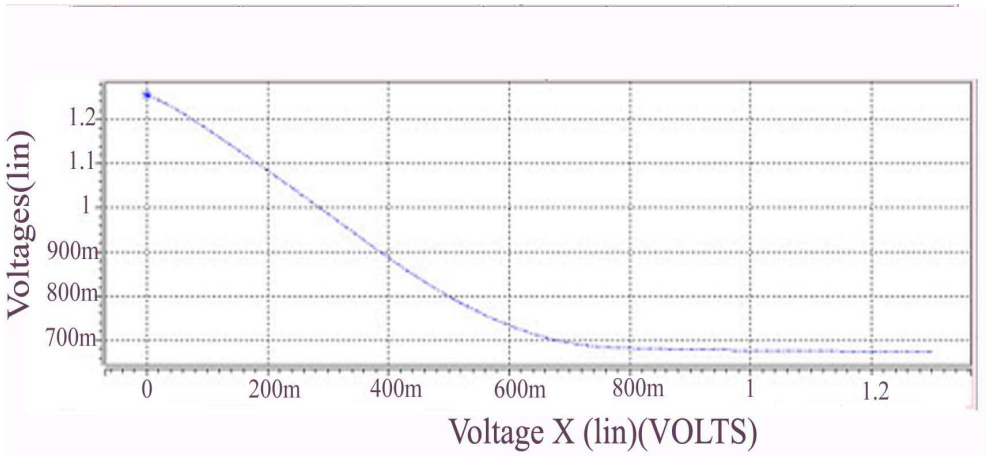


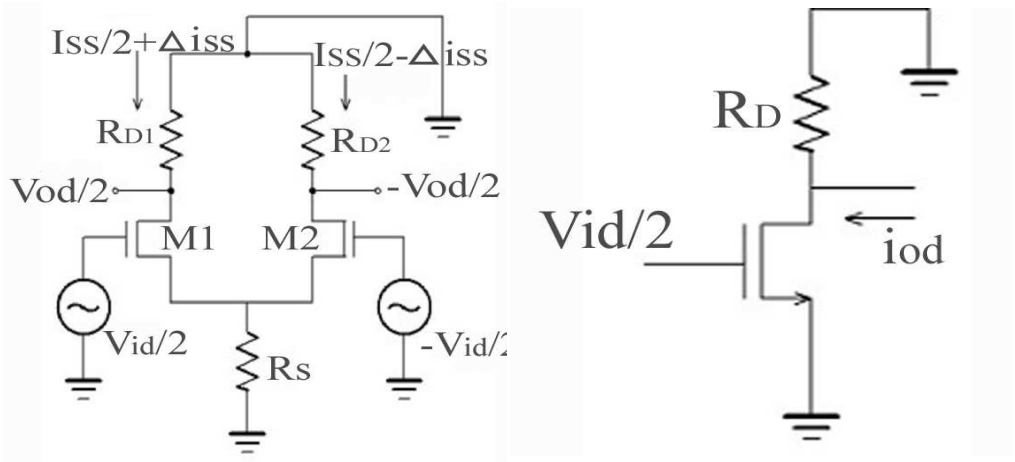
Fig 3-3(b) The Differential Mode Output VS Input Curve

2. Small signal analysis

a. Differential Mode Gain and Output Resistor

The small signal model analysis starts with putting V_{DD} to ground as shown in Fig 3-4 (a). There is no current through the source resistor R_S, so V_S is

equivalent to ground and is called virtual ground. Therefore, the left half circuit and the right half circuit are isolated by the two grounds. Because we use the same n-channel transistors and load resistors in the differential pair, the left side circuit, which consists of R_{D1} and M1, is exactly the same as the right side circuit, which consists of R_{D2} and M2. Thus we get an equivalent named half circuit, shown in Fig. 3-4 (b), to simplify the calculation; a single transistor common source amplifier with a resistor load.



(a) Small signal Model (b) Half Circuit

Fig. 3-4 Differential Pair Small Signal Equivalent Circuit

The output resistance is,

$$R_{od,Half} = \frac{\frac{V_{od}}{2}}{i_{od}} = r_{o1} // R_D \qquad (3\text{-}25)$$

$$R_{od} = \frac{V_{od}}{i_{od}} = 2 \cdot R_{od,Half} = 2 \cdot (r_{o1} // R_D) \qquad (3\text{-}26)$$

$$R_D = R_{D1} = R_{D2} \qquad (3\text{-}27)$$

Where r_{o1} is the output resistance of transistor M1; R_{od} is output resistance of the differential pair. It is the resistance looking into the circuit from output.

$R_{od,Half}$ is the half circuit output resistance.

According to the conclusion of single transistor common source amplifier with resistor load, the circuit transconductance G_m equals to device transconductance g_m. [3] P227.

$$G_m = -g_m \tag{3-28}$$

Differential mode gain A_{dm} is,

$$A_{dm} = \frac{\frac{V_{od}}{2}}{\frac{V_{id}}{2}} = -g_m(R_D // r_{o1}) \tag{3-29}$$

b. Common mode signal

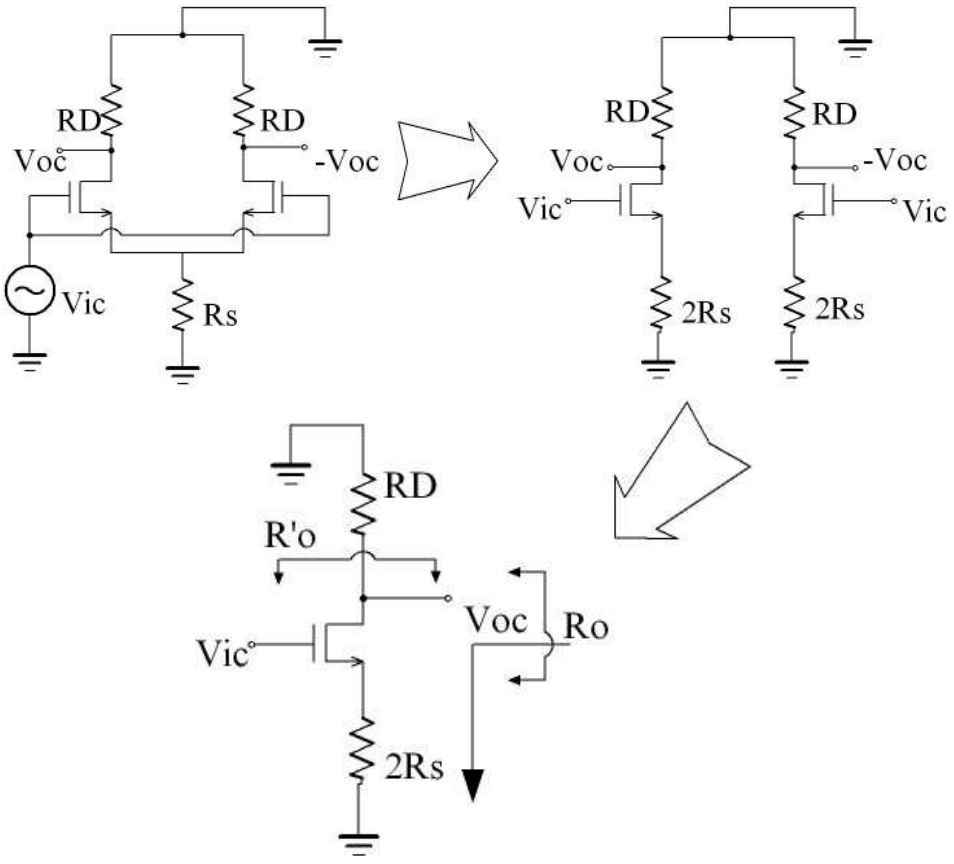


Fig. 3-5 Differential Pair Common Mode Equivalent Circuitry

We also use the half circuit module in the common mode signal analysis.

$$R'_o = (2R_s) + r_o \bullet (1 + (1+\chi) g_m \bullet (2R_s)) \qquad (3\text{-}30)$$

Where R'_o is the equivalent resistor looking from R_D, χ is the rate of change of the threshold voltage with body bias voltage, see fig. 3.5.

Assume that the bulk connects with the source. Therefore $\chi = 0$.

$$g_m \bullet R_S \gg 1 \qquad (3\text{-}31)$$

$$R'_o = (2R_s) + r_o \bullet g_m \bullet (2R_s) \qquad (3\text{-}32)$$

$$R_{oc} = R'_o // R_D \qquad (3\text{-}33)$$

$$R_{oc} = [2R_s + r_o g_m (2R_s)] // R_D \qquad (3\text{-}34)$$

According to the conclusion of single transistor common source amplifier with resistor load, the circuit transconductance G_m equals to device transconductance g_m. [3] P227.

$$G_m = -2g_m \qquad (3\text{-}35)$$

$$A_{cm} = -g_m \bullet [(2R_s + r_o g_m (2R_s)) // R_D] = \frac{-g_m R_D (2R_s + r_o g_m (2R_s))}{2R_s + r_o g_m (2R_s) + R_D} \qquad (3\text{-}36)$$

CMRR is Common Mode Reject Ratio. It is

$$CMRR = \frac{A_{cm}}{A_{dm}} = \frac{(r_o + R_D)(2R_s + r_o g_m (2R_s))}{r_o (2R_s + r_o g_m (2R_s) + R_D)} \qquad (3\text{-}37)$$

In differential input stage, we want the CMRR as small as possible.

The output of the differential input stage is

$$V_{o1} = A_{cm} V_{ic} + A_{dm} \frac{V_{id}}{2} \qquad (3\text{-}38)$$

$$V_{o2} = A_{cm} V_{ic} - A_{dm} \frac{V_{id}}{2}$$

B. Gain Stages

An op-amp get most of its gain from a gain stage. In this section we set feet

on common source amplifier (Fig. 3-6). With a proper set working set point, it may get a very large gain, I mean, large enough. The diode connection P-Channel transistor M2 acts as an active load. Fig. 3-7 is the equivalent circuit of Fig. 3-6. It is a well known configuration. We ignore the analysis and quote the conclusion from [3], pp179.

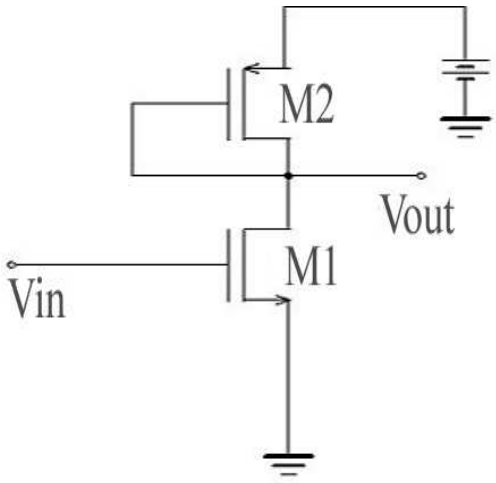


Figure 3-6 Active Load Common Source Amplifier.

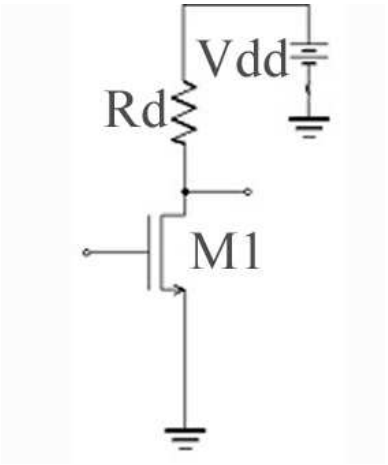


Fig. 3-7 Resistor Load simplified Circuit

To get a large output swing, we need to have smaller V_{DSAT},

1) Reduce current, because the saturation voltage is proportional to square toot of I_{DS}

$$V_{DSAT} = \sqrt{\frac{2 * I_{DS}}{K' * (\frac{W}{L})}} \qquad (3\text{-}32)$$

2) Increase W/L

3) Increase L to get a smaller λ. (λ is the channel length modulation parameter)

Fig. 3-8 shows the voltage transfer function of the common source

amplifier. The x-axis represents input voltage of gate and the y-axis represents the output voltage of drain.

When the input voltage, V_{in} is smaller than the threshold voltage V_T, the transistor M1 cutoff. V_{out} equals to V_{DD}.

With the increment of V_{in}, the transistor M1 enter the saturation region. The output is the product of input voltage V_{in} and slope of the voltage transfer function curve.

When the V_{in} is too big. The transistor works on linear region.

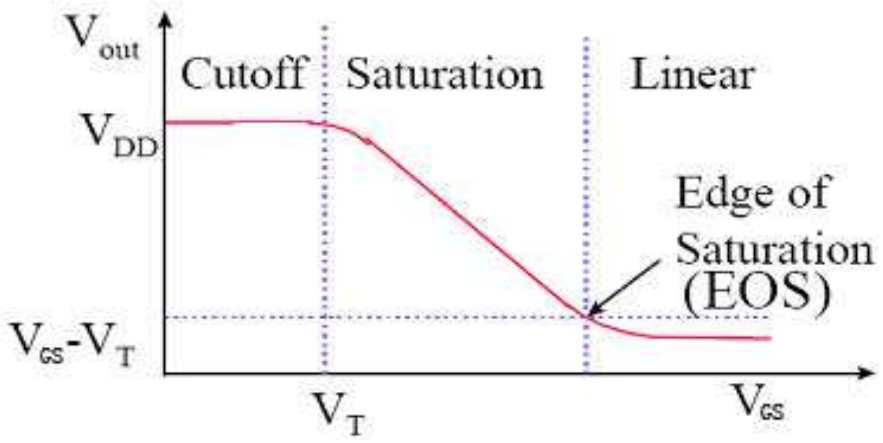


Fig. 3-8 Voltage-Transfer Function for The Common Source Amplifier

C. Output Buffers

The main design issues on output stage are large signal swing, distortion, power and efficiency.

The source follower shows on Fig. 3-9 is an option because of it high input resistance and low output resistance.

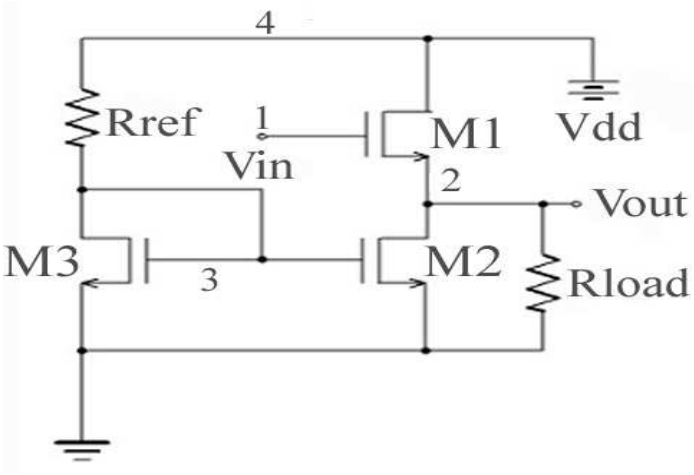


Fig 3-9 Active Load Source Follower With Bias Circuit

1. Large signal Analysis

When Vin is large enough to make transistor M1 and M2 are all in saturation, we get maximum output voltage:

$$V_{out,\max} = V_{DD} - V_{DSAT1} - V_{T,N} \qquad (3\text{-}33)$$

Where $V_{out,\max}$ is the maximum output voltage, V_{DSAT1} is the saturation voltage and the $V_{T,N}$ is the threshold voltage of N-channel transistor.

When Vin is too small, the M2 will enter a linear region because of the low voltage between drain and source. On this situation, we get minimum output voltage,

$$V_{out,\min} = 0 \qquad (3\text{-}34)$$

Where $V_{out,\min}$ is the minimum output voltage.

When the input DC signal between the two input voltage, the input equal to output because the gain of source follower is roughly 1.

The $V_{out,\max}$ and $V_{out,\min}$ are desired positive and negative swings. If the output signal is larger than positive swing or smaller than negative swing, distortion happens.

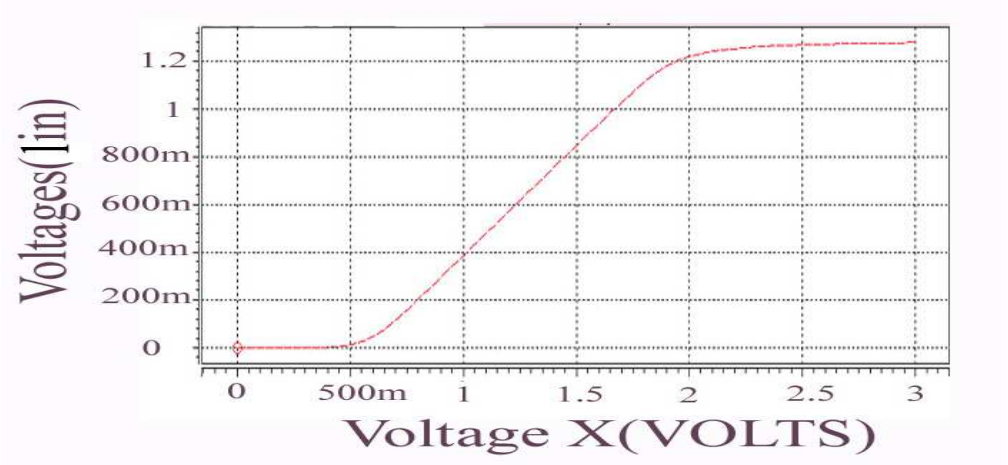


Fig 3-10 Voltage transfer characteristic of Source Follower

2. Small-signal Model Analysis

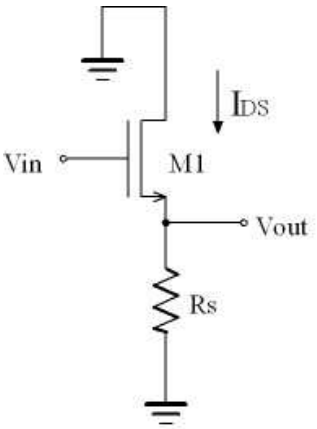


Fig 3-11 Simplified Source Follower.

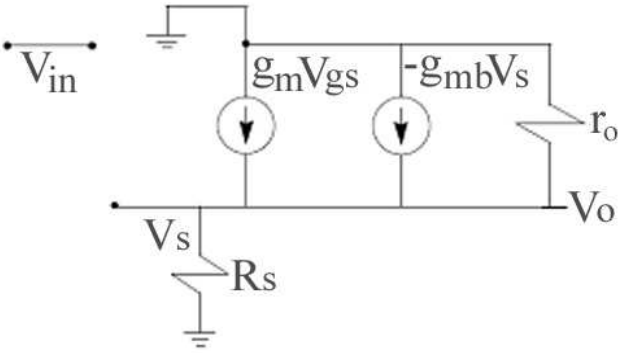


Fig 3-12 Small-signal Model of Source Follower

$$V_{gs} = V_{in} - V_s \tag{3-35}$$

$$V_{OUT} = V_s \tag{3-36}$$

$$V_s = (g_m \bullet V_{gs} - g_{mb} \bullet V_s) \bullet (r_o \| R_s) \tag{3-37}$$
$$= g_m \bullet R_s \bullet V_{in} - (1+\chi) \bullet g_m \bullet R_s$$

Where. g_{mb} is the transcondutence between source and substrate; χ is the rate of change of the threshold voltage with body bias voltage. It is a very

important factor in practise, and is defined as:

$$\chi = \frac{dV_T}{dV_{BS}} = \frac{g_{mb}}{g_m} \tag{3-38}$$

$$r_o \gg R_S \qquad A_V = \frac{V_{OUT}}{V_{IN}} = \frac{g_m R_s}{1+(1+\chi) g_m R_s} \tag{3-38}$$

$$V_s = \frac{g_m \cdot R_s \cdot V_{in}}{1+(1+\chi) \cdot g_m \cdot R_s} = V_{OUT} \tag{3-39}$$

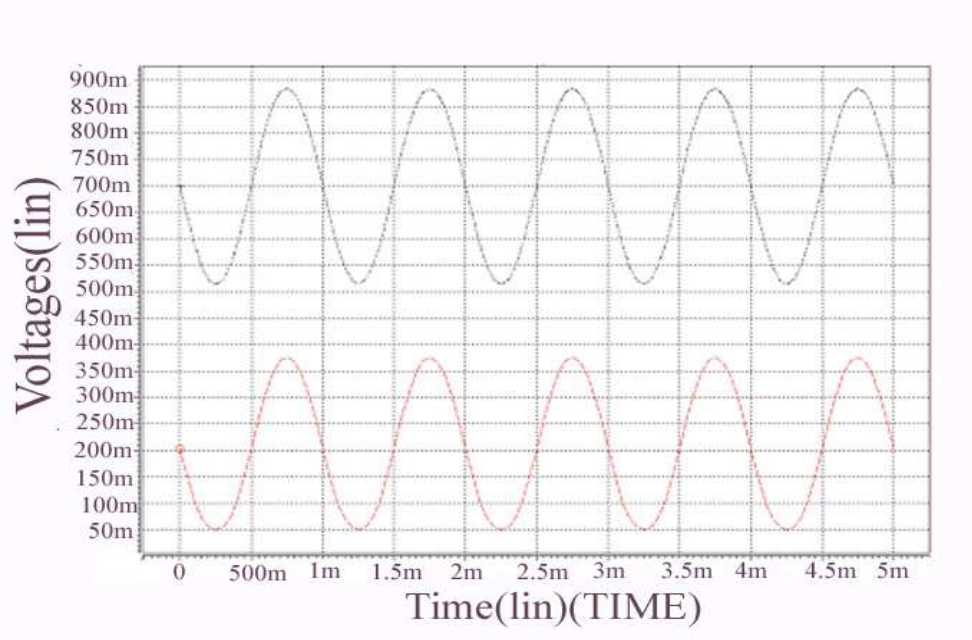


Fig. 3-13 Comparison of Input and Output Signal

Fig. 3-13 shows the input signal and output signal of the source follower. The input is on the top.

3. Distortion

The distortion is determined by the output swing, gain and the signal amplitude. If the output signal amplitude is too large to be settled between the

output swing, the distortion happens.

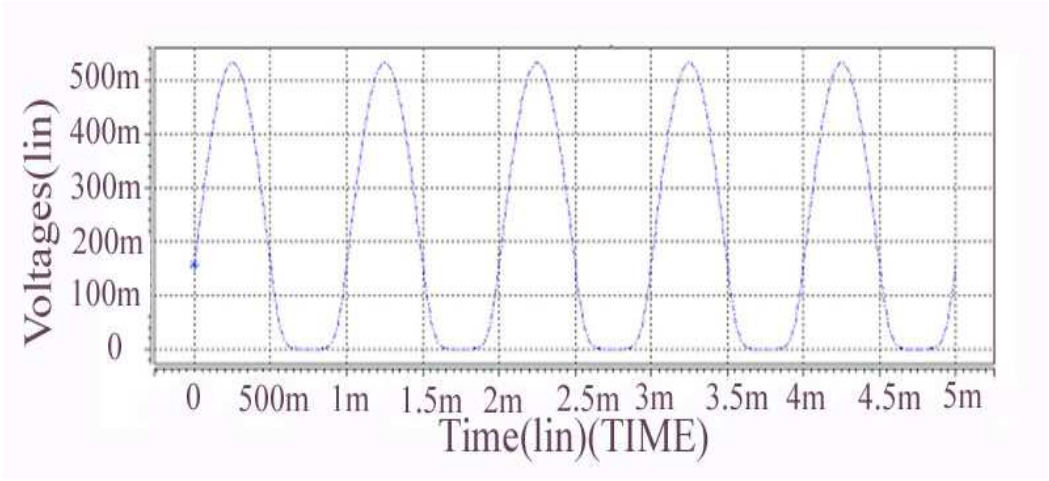


Fig. 3-14 Output Distortion

There are several methods to avoid distortion, for example, select a suitable carrier, adjust the current, scale of transistors to get a proper working point, etc.

4. Efficiency

Efficiency of the output stage is defined as the percentage of the load power consumption in total power consumption in supply.

$$Efficiency = \frac{P_{LOAD}}{P_{SUPPLY}} \cdot 100\% \qquad (3\text{-}40)$$

Where P_{LOAD} is the power into load and P_{SUPPLY} is the power from supply. A class A output stage at most can get a efficiency of 25%.

V. A Two-Stage Miller Compensation, Low voltage Op-amp

The op-amp presented here is a two-stage op-amp with miller compensation (Figure 4-1 Two-stage op-amp). Assume that the load capacitor is about 10pF. It is quite a large value. The supply voltage is about 1.4V. That is, VDD = 1.4V and VSS = -1.4V. The input swing is quite small, which is varies between -1mV and 1mV with a 1.4V load wave. And also we want to get a real-to-real output swing. A unit gain frequency band is 10MHz.

Spec	Value	Specification	Value
Gain	60dB	-3dB point	8kHz
Settling time+	300us	Settling time-	500us
ICMR+	1.0mV	Phase Margin	>45°
ICMR-	-1.0mV	Output Swing+	1.3V
Output Resistance	Infinite	Output Swing-	-1.3V
C(Load)	10pf	CMMR	>50dB

Table. 4-1 Specification of Desired Op-Amp

A. Hand calculation

Now one of the most popular design methods is to define the current firstly. According to the defined current we may scale all the parameters and other parameters such as resistance, capacitance, etc. In this case, we decide the tail

current I_5 first, which is the Drain-Source current of M5. Because the load capacitor is quite big, we increase the current to charge the load capacitor so that the settling time will not so large.

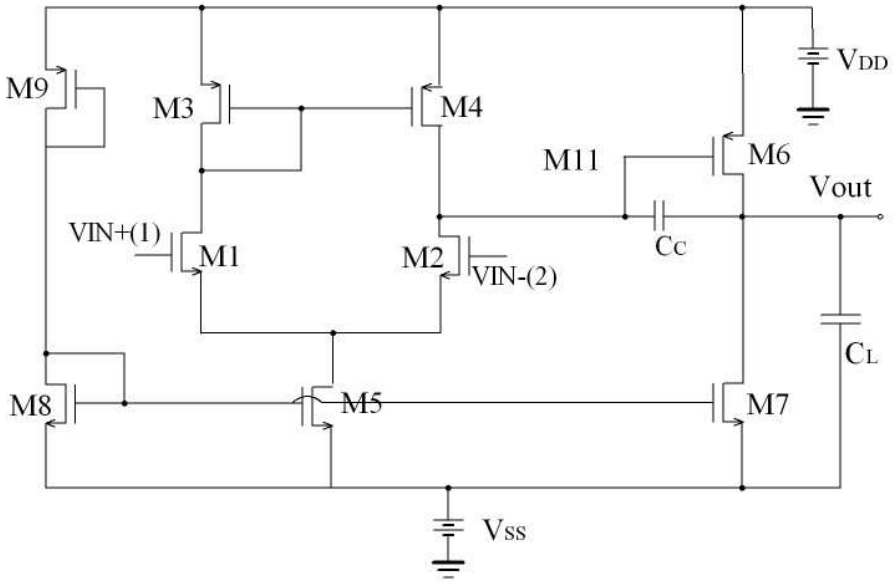


Fig. 4-1 Schematic of Two-Stage Op-Amp

The load capacitor is 10pF. And we want a phase margin at least more than 45°. Assume it is 60°. The according to the output pole, the second pore P_2 (assuming that the Right Half Plane zero z_1 is plased at or beyond ten times GB), we can get compensation capacitor,[1]

$$C_c = (\frac{2.2}{10}) * C_L \qquad (4\text{-}1)$$

Where Cc is the compensation capacitor and the C_L is the load capacitor. The load capacitor C_L is 10pF, therefore, the compensation capacitor is approximately 3pF.

$$I_5 = C_c * SR \qquad (4\text{-}2)$$

SR is the slew rate that is the ratio of output swing over setting time.

$$SR = \frac{dV_{out}}{dST} \tag{4-3}$$

Where ST is setting time. It defines the time required for the output to reach a set state after the input changes.

There are some relationship between settling time and the band. Either will be the reference of the current here. Now assemble we want our bandwidth to be 50MHz.

$$GB = \frac{1}{Time\ Constant} = \frac{1}{\tau} \tag{4-4}$$

Assume that we want a settling accuracy of 99.999%. So the Settling Time is 5 times of the time constant. That is,

$$ST = 5 \cdot \tau \tag{4-5}$$

So, from (4-4) and (4-5) we get,

$$GB = \frac{5}{ST} \tag{4-6}$$

The desired GB is 50MHz. Then we can get the settling time, $ST = \frac{5}{50e6} = 0.1us$ and the $SR = \frac{2.6\,V}{0.1us} = 26\,V/us$.

So, the tail current of the differential amplifier, I_5 is

$$I_5 = SR \cdot C_C \tag{4-7}$$

The I_5 is 54uA and the I_1, I_2, I_3 and I_4 is 1/2 of I_5. That is 27uA.

Because the GB = 50MHz, Setting Time = 0.1us.

$$g_{m1} = C_c \cdot 2 \cdot \pi \cdot GB \tag{4-8}$$

g_{m1}=942.8uS.

$$g_{m1} = g_{m2} \tag{4-9}$$

We also have,

$$g_m = \sqrt{2 \cdot k' \cdot \frac{w}{l} \cdot I_{ds}} \qquad (4\text{-}10)$$

Where k′ is about 5.67e-4; So from Equation (4-9), (4-10) and current through transistor M1 and M2, we may get the $(\frac{W}{l})_1$ =33.64, $(\frac{W}{l})_1 = (\frac{W}{l})_2$ =33.64

The ICMR+ = 1.0mV and ICMR- = -1.0mV.

$$V_{ICMR+} \le V_{DD} - V_{TP,\min} - V_{DSAT3} - V_{TN,\max} \qquad (4\text{-}11)$$

$$V_{ICMR-} \ge V_{SS} + V_{DSAT5} + V_{DSAT1} + V_{TN,\max} \qquad (4\text{-}12)$$

From(4-11) and (4-12) we can get $V_{DSAT3}$and V_{DSAT5}, with the I_5 and I_3 we can scale the transistor M3, M4 and M5. $(\frac{W}{l})_3 = (\frac{W}{l})_4$

$$\frac{w}{l} = \frac{2 \cdot I_{DS}}{k' \cdot V_{DSAT}^2} \qquad (4\text{-}13)$$

Thus, we get $(\frac{W}{l})_3 = (\frac{W}{l})_4$ =.3 and $(\frac{W}{l})_5$ =.3.

Because of a 60°phase margin, the pole of the second stage P_2 is assumed to be placed 2.2 times GB. The P_2 is given as below,

$$P_2 = \frac{g_{m6}}{C_L} \qquad (4\text{-}14)$$

$$|P_2| \ge 2.2 \cdot GB \qquad (4\text{-}15)$$

That is,

$$g_{m6} \ge 2.2 \cdot GB \cdot 2 \cdot \pi \cdot C_L \qquad (4\text{-}16)$$

Compare the equation (4-16) and (4-8) we can conclude that,

$$g_{m6} \ge 2.2 \cdot g_{m1} \cdot \frac{C_c}{C_L} \qquad (4\text{-}17)$$

For reasonable phase margin, the value of g_{m6} is approximately ten times the first stage transconductance $g_{m1.}$

$$g_{m6} = 10 \cdot g_{m1} \qquad (4\text{-}18)$$

g_{m1}=942.8uS and g_{m6}=9428uS

Then we achieve a proper mirror of the first-stage current mirror load (M3 and M4). So we get $V_{SG4} = V_{SG6}$, then

$$\frac{g_{m4}}{g_{m6}} = \frac{k_4' \cdot (\frac{W}{L})_4 \cdot V_{DSAT4}}{k_6' \cdot (\frac{W}{L})_6 \cdot V_{DSAT6}} \qquad (4\text{-}19)$$

Where V_{SG4} and V_{SG6} are voltage between source and gate of transistor M4 and transistor M6.

Approximately,

$$(\frac{W}{L})_6 = (\frac{W}{L})_4 \cdot \frac{g_{m6}}{g_{m4}} \qquad (4\text{-}20)$$

With the g_{m6} and $\left(\frac{w}{l}\right)_6$ (= 27.61u) we can get the I_6.

$$I_6 = \frac{g_{m6}^2}{2 \cdot k' \cdot (\frac{W}{L})_6} \qquad (4\text{-}21)$$

Because I_7 = I_6(=3289.4uA,) and M5 and M7 is a mirror. So

$$(\frac{W}{L})_7 = \frac{I_6}{I_5} \cdot (\frac{W}{L})_5 \qquad (4\text{-}22)$$

$(\frac{W}{l})_7$ =14.9u

Now all the transistors are scaled except M8 and M9. The M8 and M9 is a bias circuit. In most cases, people use ordinary current source. Also, a bias voltage stage is often used here.

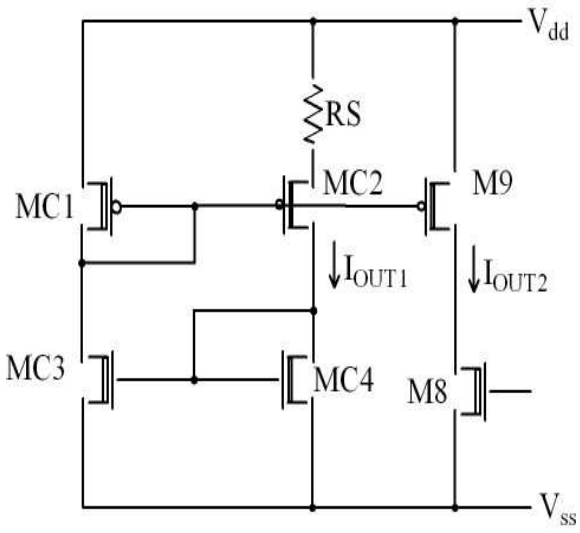


Fig. 4-2 Transistor Level Schematic Current Source

I_{OUT1} is dependent from the MC1 and MC3.

$$I_{OUT} = \frac{2}{u_{MC2} C_{OX} (\frac{W}{L})_{MC2}} \cdot \frac{1}{R_S^2} \cdot (1 - \frac{1}{\sqrt{K}})^2 \qquad (4\text{-}23)$$

Where K is the ratio of $\left(\frac{w}{l}\right)_{MC2}$ and $\left(\frac{w}{l}\right)_{MC1}$; u_{MC2}. is the mobility of Transistor M2. The MC3 and MC4 are just the same. M9 and MC2 are the same, too.

$$(\frac{W}{L})_8 = \frac{I_8}{I_5} \cdot (\frac{W}{L})_5 \qquad (4\text{-}24)$$

Anyway, we just use the schematic of Fig 4-2. The Table. 4-2 shows the final results transistor scales.

Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)
M1	33.64	M6	27.61
M2	33.64	M7	14.9

M3	1	M8	--
M4	1	M9	--
M5	1		

Table. 4-2 The Final Results of Hand Calculation

B. Optimization Design

We use simulation tools to finish optimization of the circuit. The hand calculation mentioned above is based on the Squire-Low. However, the device channel length reduced into submicron scale, the Squire-Low cannot predict the circuit performance accurately. Therefore, the computer optimal is necessary for circuit design. In this case, we take the hand calculation results as the initial guess. Then according to different specifications we defined a proper optimization method. On the another hand, the avanti tool, HSPICE provides a powerful optimization tool for users to achieve the exact circuit. Generally, there are three kinds of different optimization methods, curve fitting, goal optimization and time analysis.

In this thesis, curve fitting tool will be used to get a qualified op-amp.

The aims of optimization:

1. Scale all the transistors; use the hand calculation results as the initial guess. Get a desired AC small signal Gain at the desired frequency range, 125Hz - 8kHz.

2. Minimize the power dissipation and get a desired setting time.

According to the aims of the optimization, we divide the optimization into 2 steps. However, on most cases, one cannot get all these characteristics into the desired value, the final circuit is the tradeoff on gain, speed, power dissipation and area, etc. Therefore, we chose the most important factor that is gain in

this case as the optimal aim.

The first step is to set optimization model.

```
***
TITLE Samsung ---- A STANDARD TWO-STAGE OP AMP --- no subckt
.OPTION NOMOD NEWTOL RELMOS = 1E-5 ABSMOS = 1E-8
.MODEL OPTMOD OPT itropt = 30 CENDIF = 1.0e-9 close = 3 CUT = 2 DIFSIZ =
1e-3
+ GRAD = 1e-6 MAX = 6000 PARMIN = 0.1 RELOUT = 0.001 RELIN = 0.001
VIN+ 2 0 DC 1.1
VDD 8 0 DC 1.4
VSS 0 9 DC 0
VIN- 1 0 DC 1.1 AC 1m
CL 6 0 10P
.param LM = .18u
 M1 4 2 3 9 Mn1 W = wm1     L = LM
 M2 5 1 3 9 mn1 W = wm1   L = LM
 M3 4 4 8 8 mp1 W = WM3   L = LM
 M4 5 4 8 8 mp1 W = WM3   L = LM
 M5 3 7 9 9 mn1 W = wm5   L = LM
 M6 6 5 8 8 mp1 W = WM6   L = LM
 M7 6 7 9 9 mn1 W = wm7   L = LM
 M8 7 7 9 9 mn1 W = wm8   L = LM
 m9 7 7 8 8 mp1 W = WM9   L = LM
 CC 6 5 3p
.lib '/usr/COMLIB/L18/PRE_RULE/SPICE/L18_bsim3.lib_r1.0d' nn
.param  WM1 = OPT1(6U,3U,12U)
+       WM3 = OPT1(.3U,.18U,2U)
+       WM5 = OPT1(.26U,.18U,2U)
```

Optimization model define. We can set the accurate in the model. For example, how close the initial guess is. [7]

Description of the circuit.

```
+        WM6 = OPT1(6U,3u,12U)
+        WM7 = OPT1(2.7U,.18U,5U)
+        WM8 = OPT1(1U,.22u,8U)
+        WM9 = OPT1(1.4U,.22u,8U)
.AC data = gain1 SWEEP optimize = opt1 result = comp1 model = optmod
.measure ac comp1 err1 par(gain) vdb(6,1) minval = 55 ignor = 50
.data gain1 fre gain
1       60
1k      60
2k      60
3k      60
4k      60
5k      60
6k      58.5
7k      58
8k      57
.enddata
.ac dec 30 1 3000k
.PRINT AC V(6) VP(6)  vdb(6,1)
.END
**** optimized parameters opt1
*                                        %norm-sen          %change
 .param wm1          =    3.0416u     $     2.1012          15.8105m
 .param wm3          =  327.6352n     $     4.6891          -7.0886m
 .param wm5          =  265.9606n     $   642.1858m          51.2793m
 .param wm6          =    6.5063u     $    30.5319           1.0885m
 .param wm7          =    3.0527u     $    31.4433          -1.0570m
```

The parameters we try to optimize.

The Hspice put try different values and get the simulation result of the output node 6. Then compare the voltage of node 6 with vsup. If the relative error of these two values is smaller than the accurate requirement set in the model, the parameters will be consider as the value of the optimal result.

The desired curve of output.

.param wm8 = 712.8664n $ 15.2851 2.1743m

.param wm9 = 1.5920u $ 15.3073 -2.1713m

****

Transistor	Hand Calculation W	Optimization W
M1	6.06u	3.0416u
M2	33.64u	3.0416u
M3	180n	327.6352n
M4	180n	327.6352n
M5	180n	265.9606n
M6	4.97u	6.5063u
M7	2.7u	3.0527u
M8	--	712.8664n
M9	--	1.5920u

Table 4-3 Comparison of the Optimization and hand calculation

By these two steps, we get an optimal op-amp circuit.

Then we get into another important step, simulation.

NOTE: The syntax of model

. model mname opt <parameter = val …>

Parameters:

Name	Function	Default
CENDIF	The point when optimizing needs more-accurate derivatives. If the gradient of the results functions are less than CENDIF, Star-Hspice uses more time-consuming derivative methods. You can use values of 0.1 to 0.01in most	1.0e-9

	applications. If you use too large a value, the optimizer requires more CPU time. If you use too small a value, the optimizer might not find as accurate an answer.	
CLOSE	Initial estimate of how close parameter initial value estimates are, to the solution. CLOSE multiplies change in new parameter estimates. If you use a large CLOSE value, the optimizer takes large steps toward the solution. For a small value, the optimizer takes smaller steps toward the solution. Close ranges from 0.01 (very close parameter estimates) to 10 (rough initial guesses). If CLOSE is greater than 100, the steepest descent in the Levenburg-Marquardt algorithm dominates. If CLOSE is less than 1, the Gauss-Newton method dominates.	1.0
CUT	Modifies CLOSE, depending on how successful iterations are, toward the solution. If the last iteration succeeds, descent toward the CLOSE solution decreases by the CUT value. If the last iteration was not a successful descent to the solution, CLOSE increases by CUT squared. CUT drives CLOSE up or down, depending on the relative success in finding the solution. The CUT value must be >1.	2.0
DIFSIZ	Increment Change in a parameter value, for gradient calculations $(\Delta x = \mathrm{DIFSIZ} \cdot \max(x, 0.1)$. If you specify delta in a .param statement, then $\Delta x = delta$.	1e-3
GRAD	Represents possible convergence, if the gradient of the RESULTS function is less than GRAD. Most applications use values of 1e-6 to 1e-5. Too large a value can stop the optimizer before finding thebest solution. Too small a value requires more iteration.	1.0e-6
ITROPT	Maximum numberof iterations. Typically, you need no more than 20-40 iterations, to find a solution. Too many iterations can imply that the RELIN, GRAD, or RELOUT values are too small.	20
LEVEL	Selects an optimizing algorithm. Currently, the only option is LEVEL-1, a modified Levenburg-Marquardt algorithm.	1
MAX	Sets the upper limit on CLOSE. Use values >100. (接近上限)	6000
PARMIN	Allows better control of incremental parameter changes, during error calculations. This produces more control over the tradeoff between simulation time and optimization result accuracy. To calculate parameter increments, Star-HSPICE uses the relationship:	0.1

	$\Delta par\_val = DIFSIZ \cdot MAX(par\_val, PARMIN)$	
RELIN	Variation in the relative input parameter, for convergence. If all optimizing input parameters vary by no more than RELIN between iterations, the solution converges. RELIN is a relative variance test, so a value of 0.001 implies that optimizing parameters vary by less then 0.1%, from one iteration to the next.	0.001
RELOUT	Represents the variance in the relative output RESULTS function, for convergence. For RELOUT = 0.0001, the difference in the RMS error of the RESILTS functions, vary less than 0.001.	0.001

Table 4-5 Parameters of optimization mode

C. Simulation & Measurement

The simulation and measurement include: open loop gain, open loop frequency response (including the phase margin), input offset voltage, common-mode gain, power-supply rejection ratio, common mode input and output voltage ranges, open loop output resistance, and transient

1. DC Transfer Characteristic (Appendix A.1)

The first specification to be measured is the DC transfer characteristic. Also, thistest is used to determine the input offset voltage and power dissipation. Because we use the single end supply in this op-amp, the operating voltage to both end of the input will be decided instead of the offset voltage.

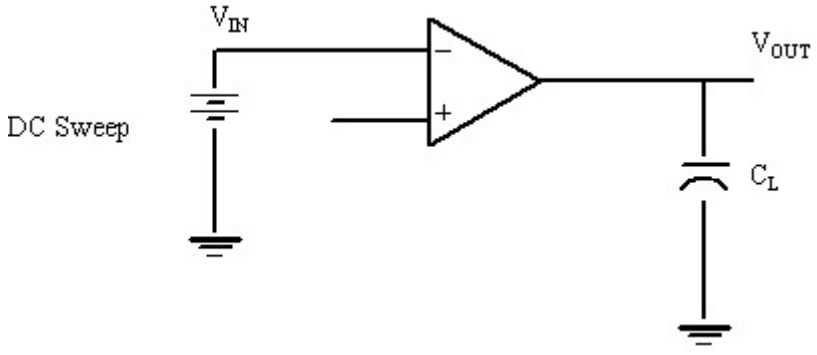


Fig. 4-3. Test Configuration for DC Transfer Characteristic Setup

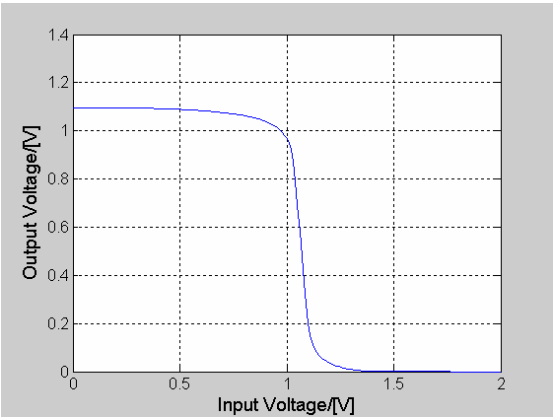


Fig. 4-4. DC Transfer Characteristic of Open-Loop Op-Amp

From the measurement we can see the operating voltage of both end is 1.2V.

2. Open-Loop Gain and Frequency response (Appendix A.2)

The open-loop gain is,

$$A_v = A_I \cdot A_{II} \tag{4-25}$$

A_I is the gain of the first-stage, a differential input stage. The A_{II} is the gain of the second stage. If the optimization is not good enough to satisfy our demand for the large gain, we can adjust both of them to enlarge the gain. Here we increase the gain of the second-stage, A_{II}. The second-stage is a current load common source output stage. The gain is,

$$A_{II} = R_{OUT2} \bullet G_{M2} \tag{4-26}$$

Keep the current as a constant, or we have to adjust all the circuit.

$$G_{M2} = -g_{m6} \tag{4-27}$$

Where

$$g_{m6} = \sqrt{2 \cdot k'_p \cdot \left(\frac{w}{l}\right)_6 \cdot I_{DS6}} \tag{4-28}$$

So, if we increase the $\left(\frac{w}{l}\right)_6$, the A_{II} will increase, too. Let's have a look at the pole P_2 of the second stage. According to Equation (4-14), if we increase g_{m6}, the second-stage pole will be greater. That means the pole is push to a higher frequency. It will not be a trouble in this case. So we can increase the gain via increase the size of the transistor M6. The M7 should change with the M6. Keep all other parameters as constants and optimize the transistor M6's scale.

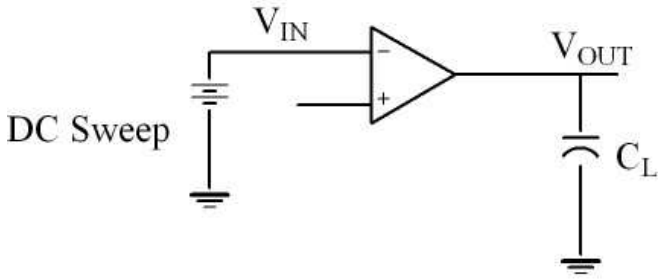
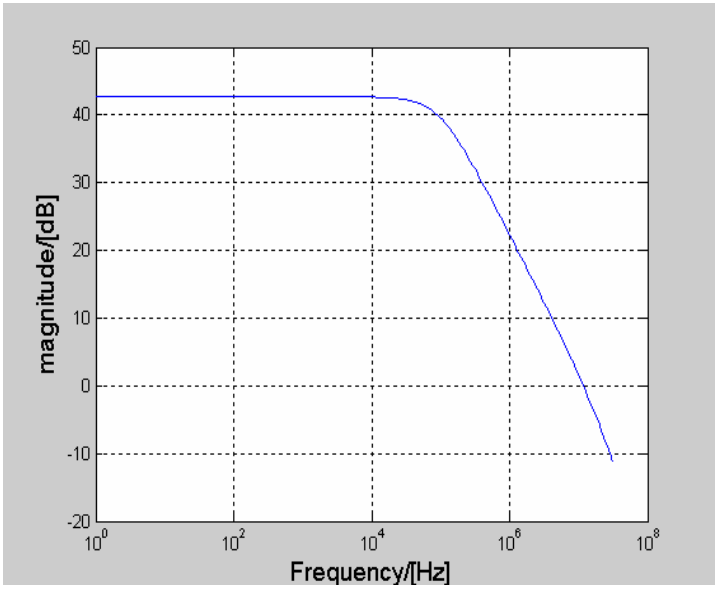
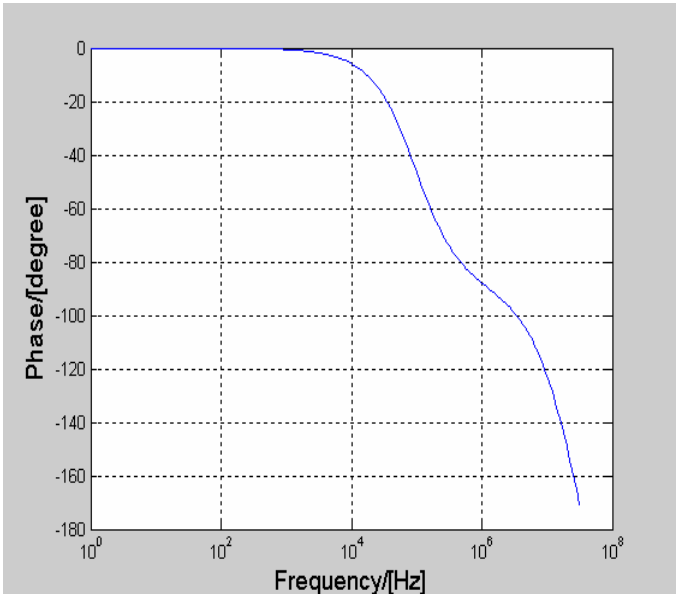


Fig. 4-5. Test Configuration for Open-Loop Frequency Response

The result is not so good. The gain is only about 44dB. It is because we use short channel devices in this design.



(a) Magnitude-Frequency Response.



(b) Phase-Frequency Response

Fig. 4-6 Bode Plot of The Two-Stage Op-amp

3. Output Swing. (Appendix A.3)

Output swing is limited by the transistor M6 and M7. We should get a overdrive voltage as low as possible. However we should know that the gain needs a large current via M6 and M7. That will be another tradeoff between the gain and the output swing.

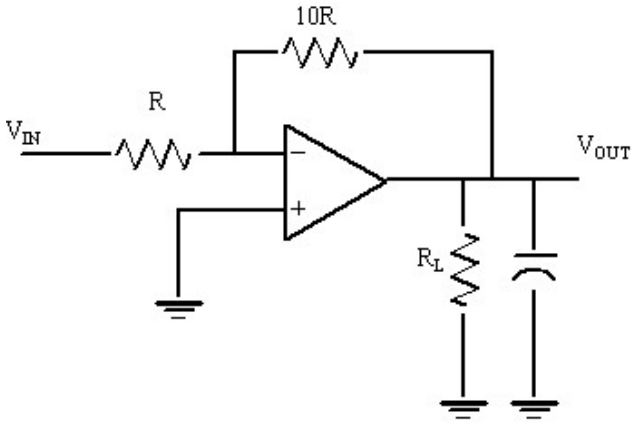


Fig. 4-7 Test Configuration for Output Swing

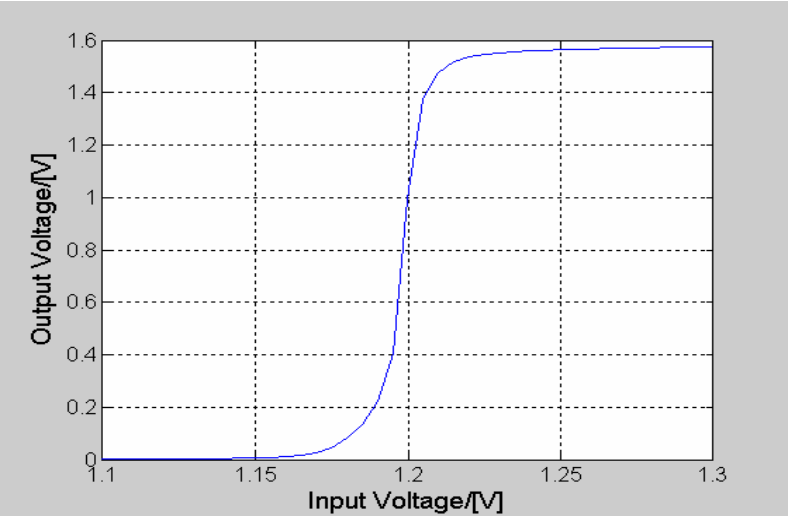


Fig. 4-8 Output Swing

When the positive is supplied by 1.2V, the offset voltage is very small, about 0.00001V. So we just ignore the offset voltage. However, practically, the offset voltage varies with the temperature and noise and we should keep an eye on it.

4. Settling Time (Appendix A.4)

The settling time of a two-stage standard CMOS op-amp in this design is affected by two different parameters. Both the phase margin and the slew rate will alter the settling time.

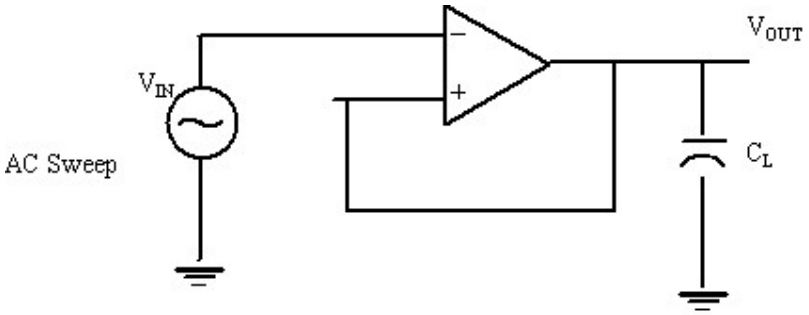


Fig. 4-9. Test Configuration for Settling Time

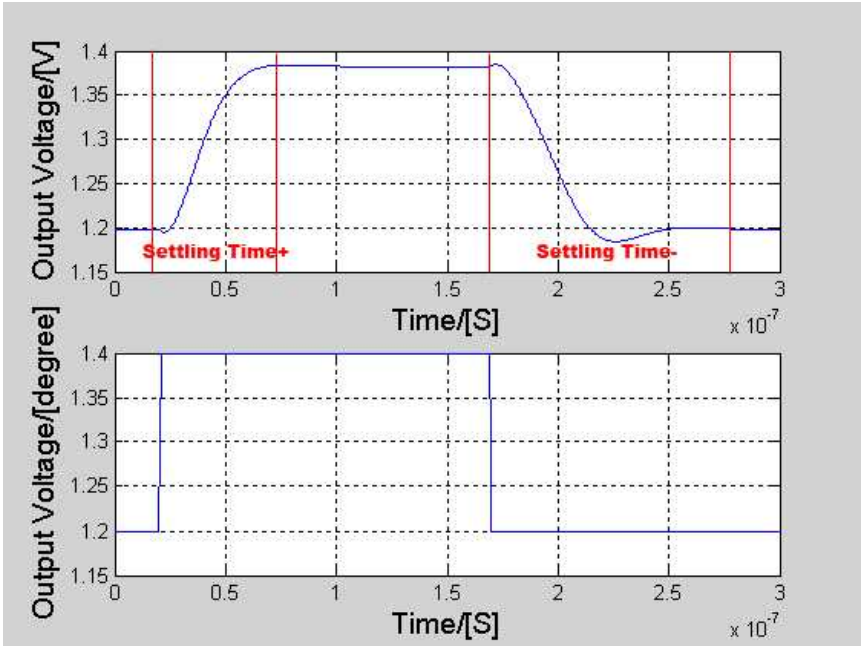


Fig. 4-10 Settling Time

From Fig 4-10 we can see, the positive settling time is about 0.0818us and the negative settling time is about 0.114us. The value is much larger than the design requirement.

5. Common-Mode Range (CMR) (Appendix A.5)

We have proved that the CMRR relates to the transistor M5 and M3. To achieve a large gain, the overdrive voltage should be very low. Figure 4-11 shows the configuration of testing the CMR.

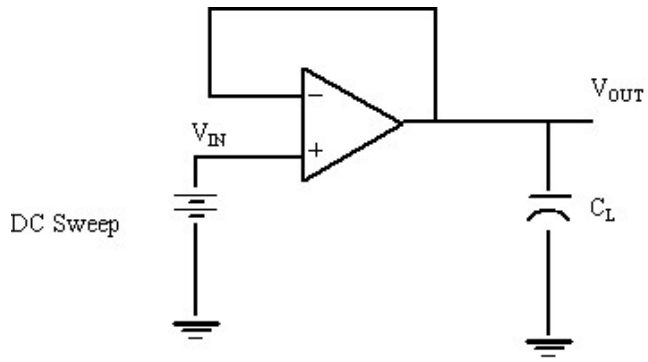


Fig. 4-11 Test Configuration for CMR

Fig 4-11 shows the result. The input common mode Range is from 0V to 1.4V.

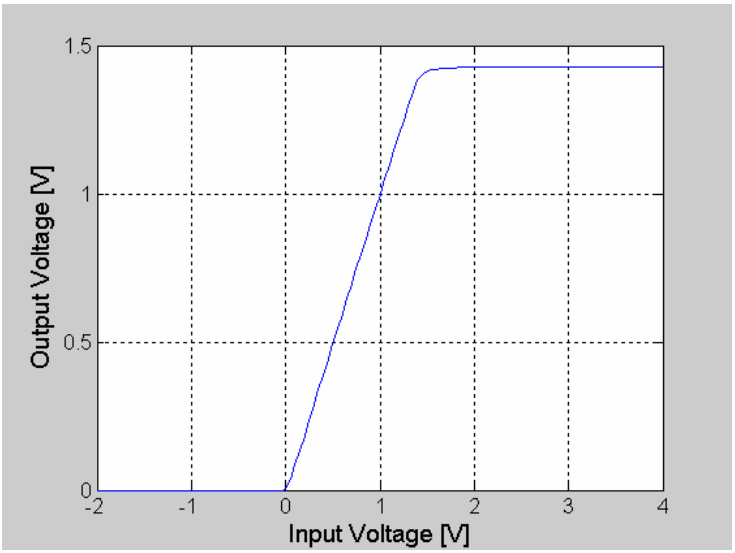


Fig. 4-12 Common-Mode Range CMR

6. Common-Mode Rejection Ratio (CMRR) (Appendix A.6)

The common-mode rejection ratio (CMRR) is predominantlycontrolled by the resistance seen looking into the current sink of M7. CMRR was verified using the circuit configuration shown in Figure 4-13 This configuration provides a method to directly calculate CMRR by finding the ratio V_{cm}/V_{out}. This direct

calculation of CMRR is very beneficial because it can then be plotted directly in the frequency domain to obtain the CMRR frequency response.

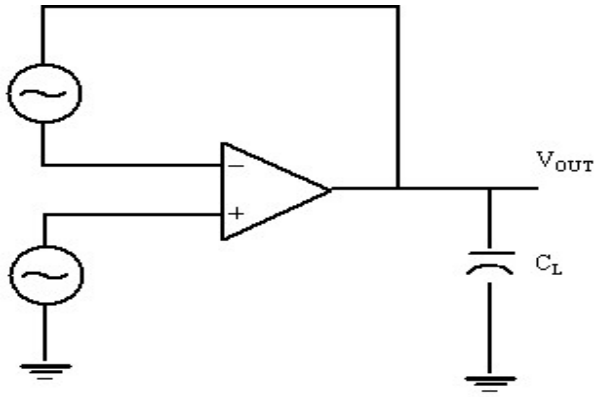


Fig. 4-13 Test Configuration for the CMRR

7. Power Supply Rejection Ratio (PSRR) (Appendix A.7)

The power supply rejection range shows the power supply dependence of the op-amp. We want a larger power supply rejection ratio because that means the op-amp is more independent to the power supply. The PSRR can be got via changing supply voltage and watching the change of the output. The Figure 4-14 shows the test configuration of thePSRR. It should be divided into two steps. First, keep V_{ss} as a constant and AC sweeps V_{dd}. Then get the ratio of $V_{out}/\triangle V_{dd}$, that is PSRR+. Second, keep V_{dd} as a constant and AC sweeps V_{ss}. Then get the ratio of $V_{out}/\triangle V_{ss}$, that is PSRR-.

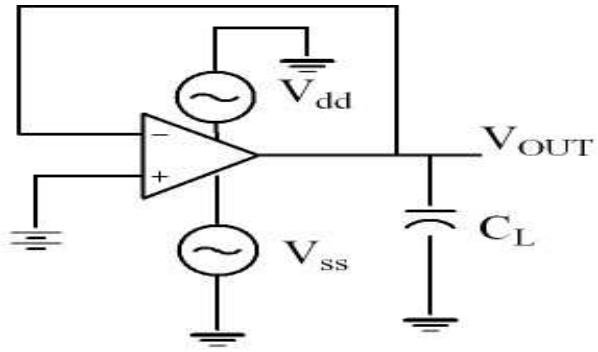
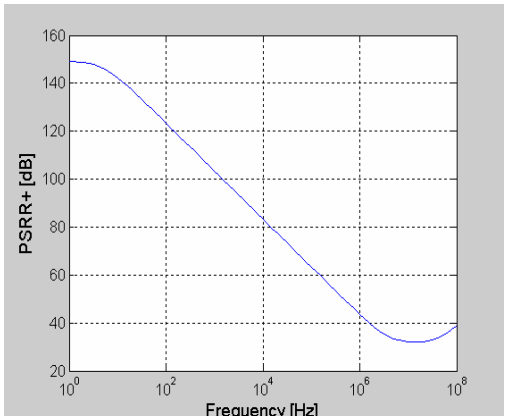
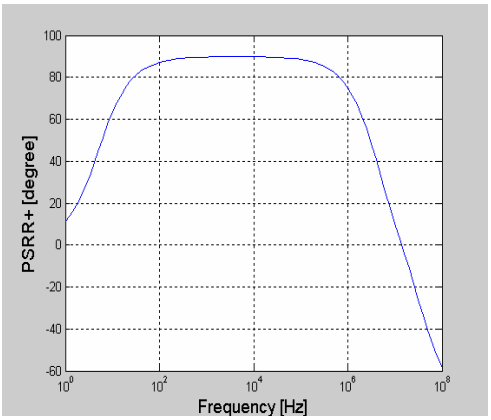


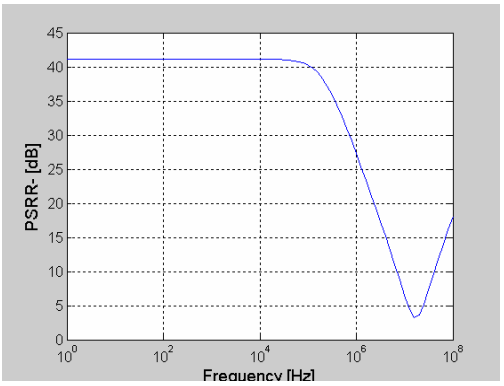
Fig. 4-14 Test Configuration for PSRR



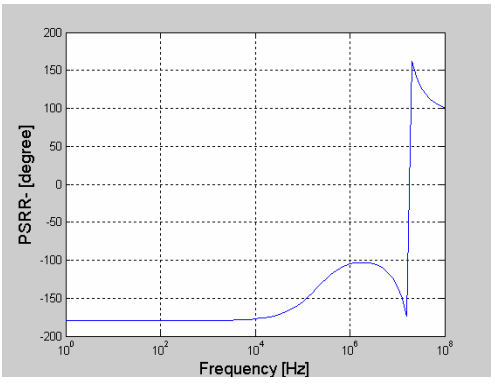
(a) PSRR+ Magnitude-Frequency Response.



(b) PSRR+ Phase-Frequency Response.



(c) PSRR- Magnitude-Frequency Response.



(d) PSRR- Phase-Frequency Response.

Fig. 4-15 PSRR Bode Plot

Spec	Designed Value	Simulation Value
Gain	60dB	44.6dB
Settling time +	.01μs	.08μs
Settling time -	.01μs	.11μs
ICMR +	+ 1.0mV	1.4V
ICMR -	0mV	0mV
CMMR	50dB	68.89dB
Input Resistance	Infinite	1.0e20
PSRR+	>60dB	140dB
PSRR-	>60dB	40dB
Output Swing+	+1.8V	1.6V
Output Swing_	0V	0V
Output Resistance	--	6.3583k
Input Resistance	Infinite	1.0e20
Total Power Dissipation	--	1.46mWatt

Table 4-6 Comparison on Specifications of the Op-amp

D. Summary

In this section, we designed a two-stage miller compensation op-amp. It is a standard op-amp and is wildly used. The design begins with hand calculation. Though the square low is not so accurate for the sub-micrometer models, it helps to scale the circuit more efficiently. What's more, hand calculation provides a clear relationship and change tendency among all the parameters. The optimization tools that HSPICE provides are powerful, though it is not so perfect. The reduction of the channel length makes it possible to use it in a

low voltage surrounding. However, the low supply voltage also limits the gain. Later we will discuss the CMOS analog design with low supply voltage and low power consumption.

VI. Single-Supply, Low Voltage Op-amp

The calculation described in former section is mainly based on square law. It is quite precise when the channel length is not very short (longer than 1um). With the reduction of the device size, short channel effects on CMOS transistors appear. These short channel effects, such as a lower but unstable threshold voltage and a changing mobility, make the square law unfit for the prediction of the circuit performance. The only effective and reliable tool left is the spice simulation program. Therefore, a new method which takes advantage of spice simulation to get a desired circuit is introduced into our design. Here is a simple example.

[Ex.1] Design a Common source amp, Av0 > 100, unit gain frequency f_u = 100MHz, for C_l = 5pF.

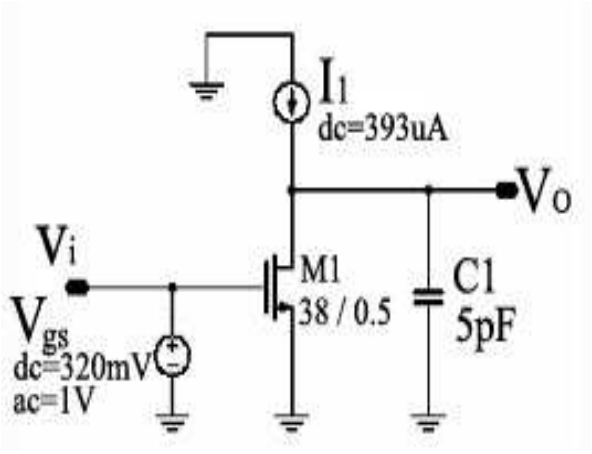


Fig. 5-1 A Common-Source Amp.

Solution:

Because Av0 > 100, (a large gain) -> L = 0.5u

$G_m = 2 \cdot \pi \cdot f_u \cdot C_l = 314mS$

$V^* = 250mV$

$$I_D = \frac{g_m V^*}{2} = 393uA$$

The V^* is the minimum voltage drop between drain and source. It is larger than the saturation voltage, V_{DSAT}, which defined in square law and smaller than the real voltage drop between drain and source.

Then we refer to a model card got from simulation. In theory you may choose a transistor model card of any size. In this example, I use a transistor model card with W/L = 10/0.5.

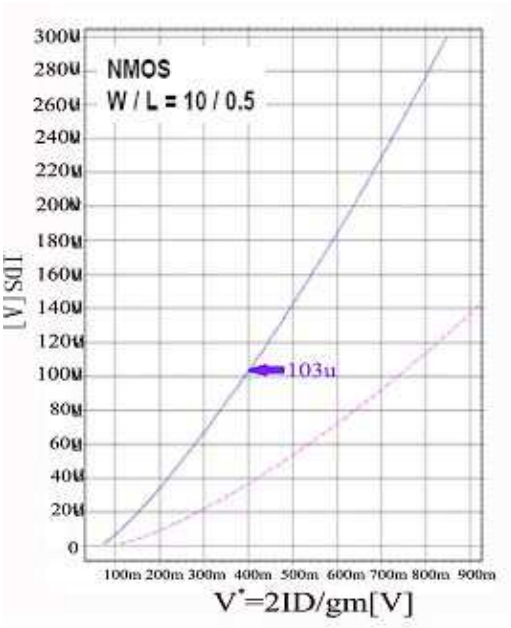


Fig 5-2 A Model Card with W/L = 10/0.5

Fig.5-2 shows an example of model card. It is a NMOS transistor with a W/L of 10/0.5. The x-axis is V^* and the y-axis is current. With the V^* = 250mV, We get a current of $I_D = 103uA$ (from simulation)

$$W/L \propto I_{DS}$$

$$\frac{10u}{x} = \frac{103uA}{393uA}$$

So, x = 38um.

The x is the width of the NMOS transistor we want.

After the discussion of design methodology, we start the job on operational amplifier.

The operational amplifiers used in hearing aids are specially designed to meet the requirements of low voltage, single-supply, low power dissipation, high gain, etc. Because the input signal from microphone is very small, less than .01mV,

the op-amp is designed to be very sensitive to such a tiny signal. On the otherhand, the op-amp should have a rail-to-rain output swing as well as a very low output impedance to avoid distortion and waste of power.

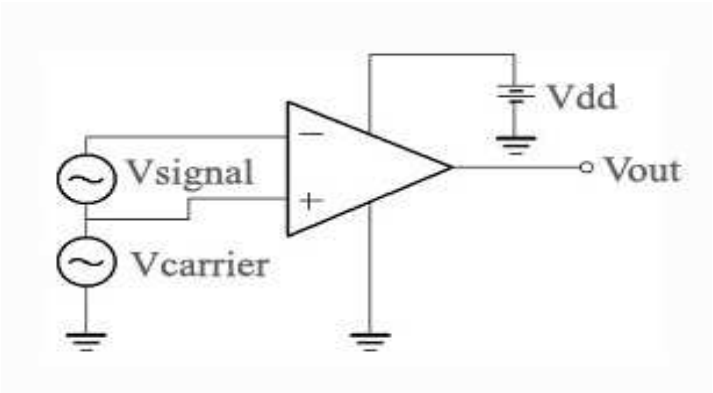


Fig. 5-3 Application Schematic

The op-amp consists of three stage, input stage, gain stage and output stage. The input stage is an N-channel differential pair. The gain stage is a current load common source P-channel transistor. A class A source follower acted as an output stage to deal with a very small resistor load.

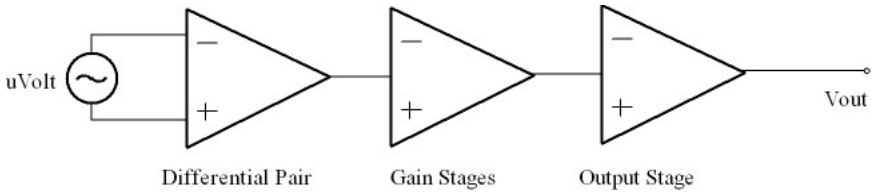


Fig. 5-4 Diagram of A Multi-Stage op-amp

A. Input Stage

The input signal is less than 0.01mV. That is,

$$V_c - 0.01mV < V_c < V_c + 0.01mV \qquad (5\text{-}1)$$

$$V_{in} \geq V_{DSAT5} + V_{DSAT1} + V_{TN} \quad (5\text{-}2)$$

$$V_{in} \leq V_{DD} - V_{DSAT4} - V_{TN} \quad (5\text{-}3)$$

Where V_{DSAT5} V_{DSAT4} and V_{DSAT1} are the saturation voltage of transistors M5, M4 and M1. V_{TN} is the threshold voltage of N channel transistor. So in the design, we do not need to take cascode in input stage to extend the common mode input range (ICMR). A regular N-channel differential pair input stage provides enough ICMR for the op-amp. We chose Vc = 0.7V. Fig 2 shows the transistor level schematic. Transistors Mb1, Mb2 and the resistor Rref compose a voltage divider to provide a carrier for the circuit. Node 6 is the output to the next stage. Vsignal is the input signal.

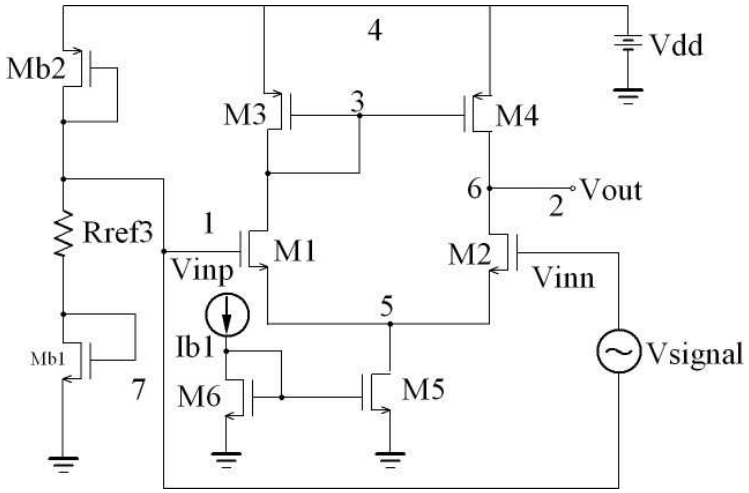


Fig. 5-5 Transistor Level Schematic of Input stage

$$A_{dm} = \frac{\frac{V_{od}}{2}}{\frac{V_{id}}{2}} = -g_m(R_D // r_{o1}) \quad (5\text{-}4)$$

Equation. (4) state the relationship among circuit parameters. Where V_{od} is the differential mode output voltage and V_{id} is the differential mode input voltage. g_m is the transconductance of transistor M2, M1. R_D is the equivalent load resistance. To improve the gain, we may increase the gate length of the M1 and M2, the ratio of W/L or reduce the current from current source Ib1.

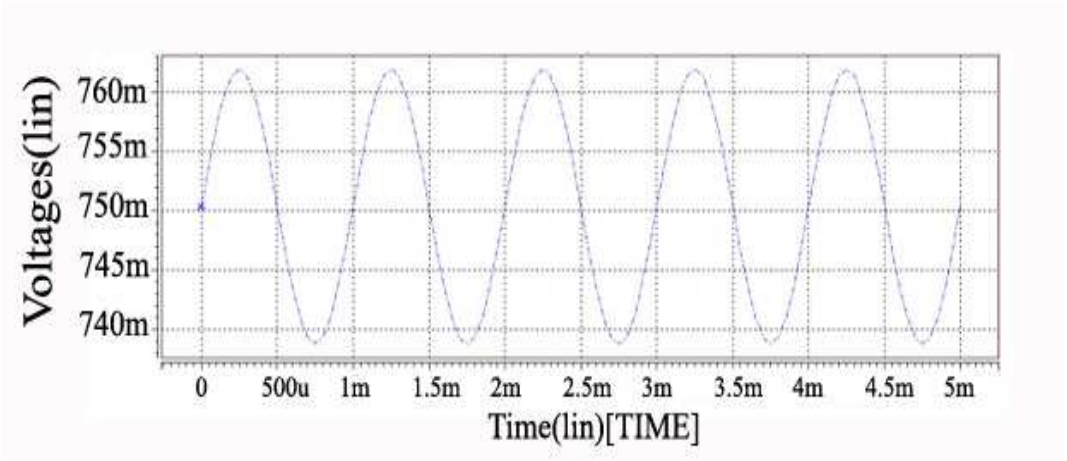


Fig. 5-6 (a) AC Output Wave of Input Stage. (Appendix A.8)

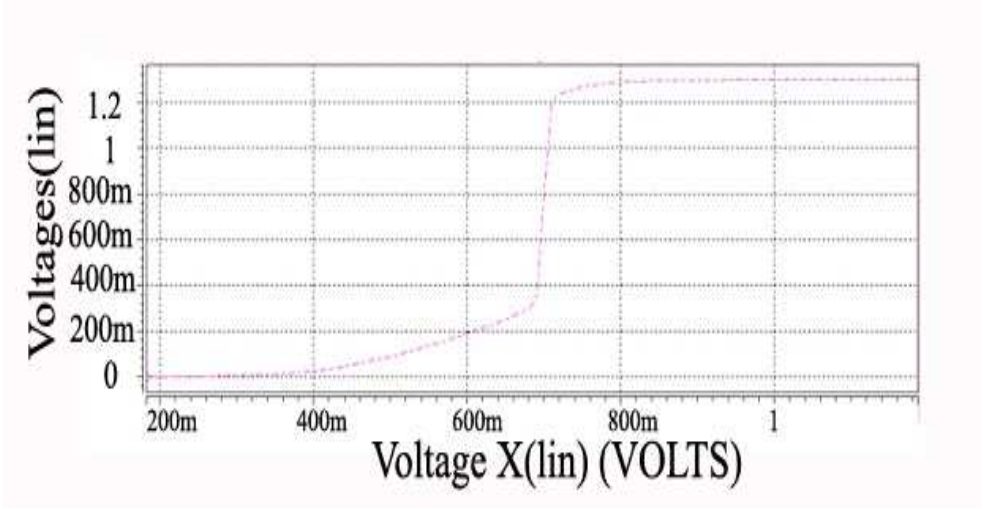


Fig. 5-6 (b) DC Output Wave of Input Stage.

Transistor	W [μm]	L [μm]
M1	16.30	1.00
M2	16.30	1.00
M3	23.74	1.00
M4	23.74	1.00
M5	10.63	1.00
M6	10.63	1.00
M7	10.21	1.00

Table 5-1 The Scale of Transistors.

Vout/Vin	115.97
Input Resistance	1.000e+20
Output Resistance	565.317k

Table 5-2 Small-Signal Transfer Characteristics of Input Stage

B. Gain Stage

The gain stage used in the design is a regular active load common source amplifier. M11, M10, Rref2 and M9 compose a current source. The diode connection transistor M11 could be regarded as a large resister so that we can reduce the size of the resistor, Rref. M10 is exactly the same as M9 so that the current through M11 equals to the current through the transistor M8. Vinput is the output from input stage. The hearing aids are only interested in the low frequency input signals which covers between 20 Hz and 8kHz. We found there is no phase shift when the input frequency is less then 10E4 Hz even we did not do any frequency compensation. Fig. 5shows the structure of

the gain stage.

The gain of active load common source transistor is determined by the transconductance of the transistor M8 and the equivalent load resistance, Equation. (5-4). So we can increase the gate length, the W/L to get a larger gain. Reduce current also help to do so. Fig. 5-6 show the frequency response of the gain stage.

Table 2 shows the small signal transfer characteristics of the gain stage. It got a gain of 92.78 at low frequency.

Vout/Vin	92.78
Input Resistance	1.000e+20
Output Resistance	466.102k

Table 5-3 Small-Signal Transfer Characteristics of Gain Stage (Appendix A.9_a)

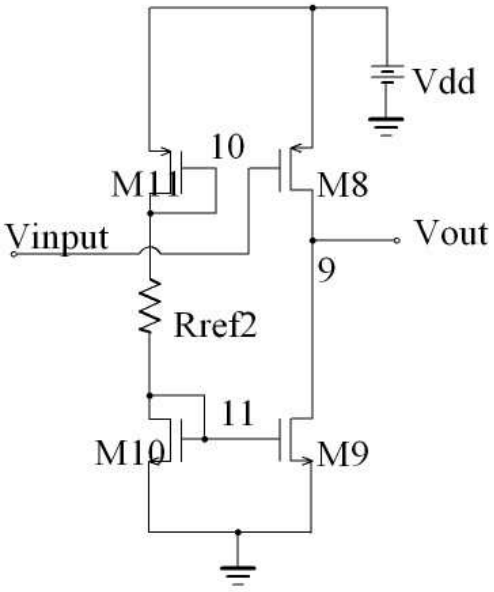


Fig. 5-7 Transistor Level Schematic of Gain stage

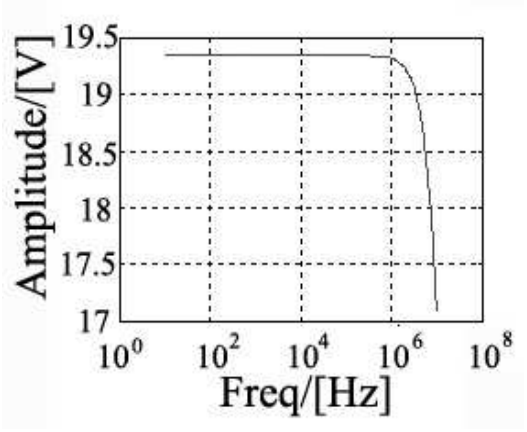


Fig. 5-8 (a) Amplitude-Frequency Response

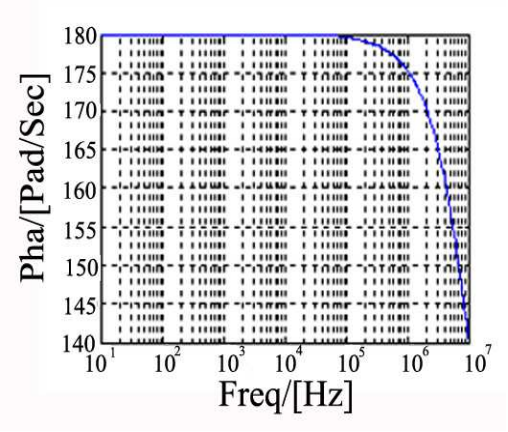


Fig. 5-8 (b) Phase-Frequency Response (Appendix A.9_a)

C. Output Stage

The desired gain of the op-amp is 80dB. The input signal is less than 0.01mV. The output is

$$V_{oc} - 100mV \le V_{OUT} \le V_{oc} + 100mV \qquad (5\text{-}5)$$

So a source follower was chosen to be the output stage. (Fig. 5-7)

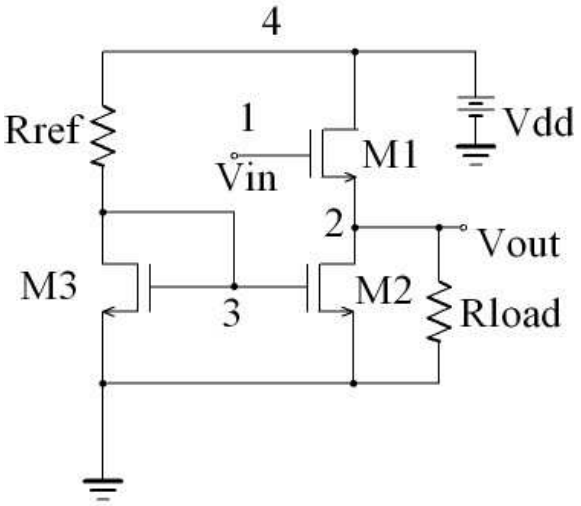


Fig. 5-9 Transistor Level Schematic of Output Stage

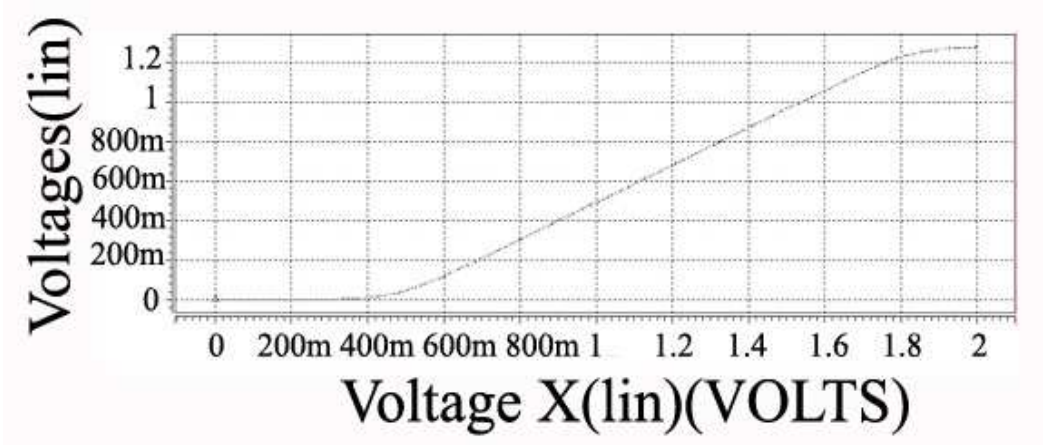


Fig. 5-10 (a) DC Transfer Characteristic

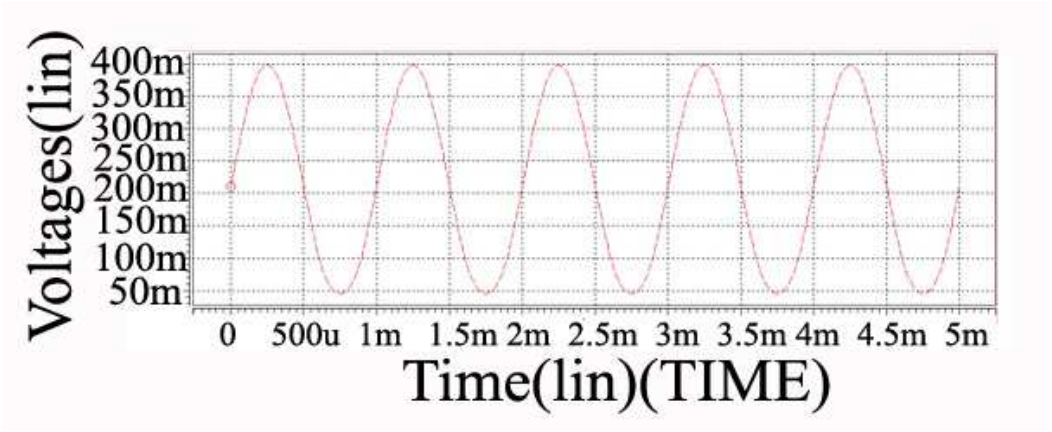


Fig. 5-10 (a) AC Transfer Characteristic

Vout/Vin	978.2m
Input Resistance	1.000e+20
Output Resistance	28.23k

Table 5-4 Small-Signal Transfer Characteristics

D. Full Circuit Simulation and Test

Fig. 5-9 shows the full schematic of the op-amp. In this schematic, the voltage divider which produce the carrier was not included. The transistors M7, M6, M5 and resistor Rref compose a current source. M1, M2, M3, M4 and M5 consist a N-Channel differential pair. M5 provided a tail current. The transistor M8 is a common source amplifier with a current source load. The transistor M10 is a source follower. All these parts are analyzed and simulated on former section. Here we tested the specifications of the op-amp.

The specifications we interested in are gain, phase margin, ICMR, Common Mode Reject rang (PRSS), output swing, Common Mode Rejection Range (CMRR) and Settling time.

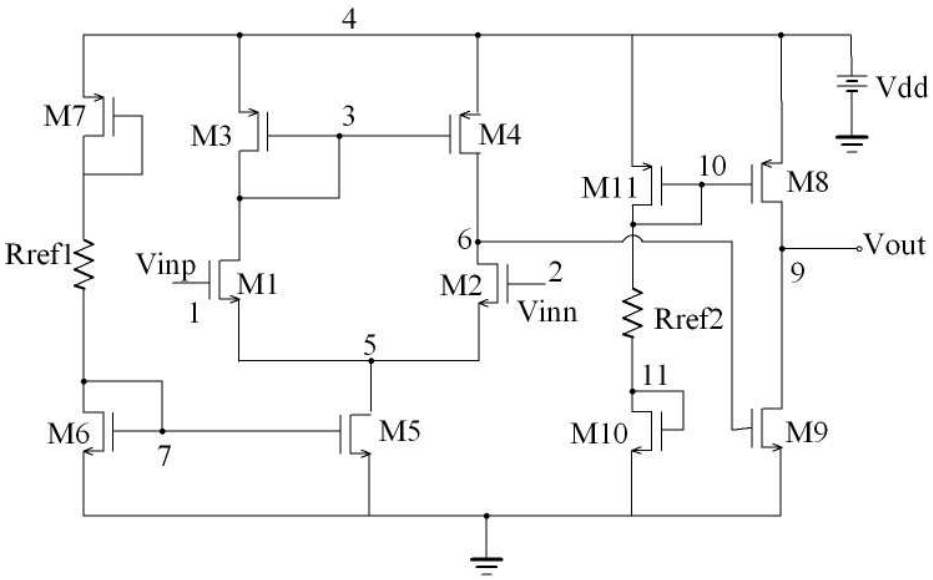


Fig. 5-11 The Complete Schematic of the Op-amp

1. Frequency response

Table 5-5 and Fig. 5-12 show frequency response of op-amp. The gain is 82dB. There is enough phase margin to deal with low frequency with

acceptable phase shift.

Vout/Vin	12.25k
Input Resistance	1.000e+20
Output Resistance	25.04k

Table 5-5 Small-Signal Transfer Characteristics

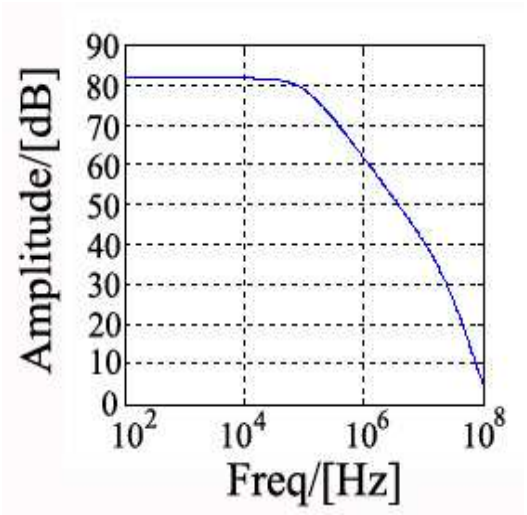


Fig. 5-12 (a) Amplitude-Frequency Response

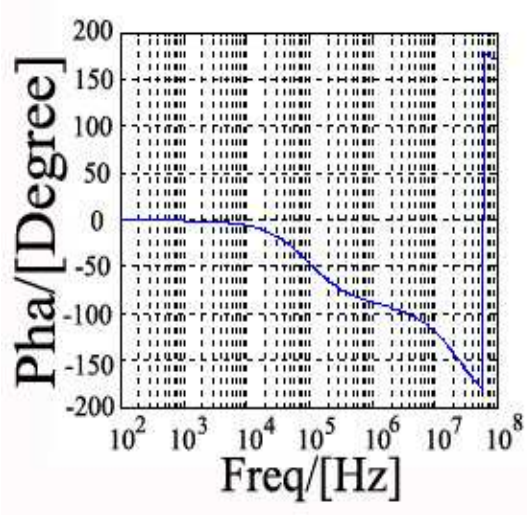


Fig. 5-12 (b) Phase-Frequency Response (Appendix A.11)

2. CMRR

CMRR, Common Mode Reject Range, is defined as Equation. (5-5). The Acm is common-mode gain and the Adm is the differential-mode gain. In fig. 11(a), we use the absolute value.

$$CMRR = \frac{A_{CM}}{A_{DM}} \qquad (5\text{-}5)$$

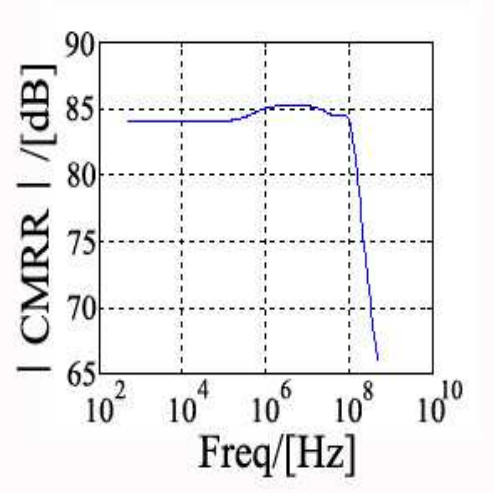


Fig. 5-13 (a) CMRR Amplitude-Frequency Response.

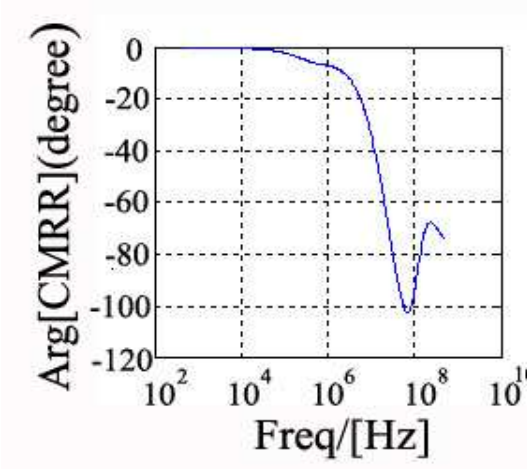


Fig. 5-13 (b) CMRR Phase-Frequency Response. (Appendix A.12)

3. Output Swing

The output is between 0V and 767mV when the input varies in the ICMR.

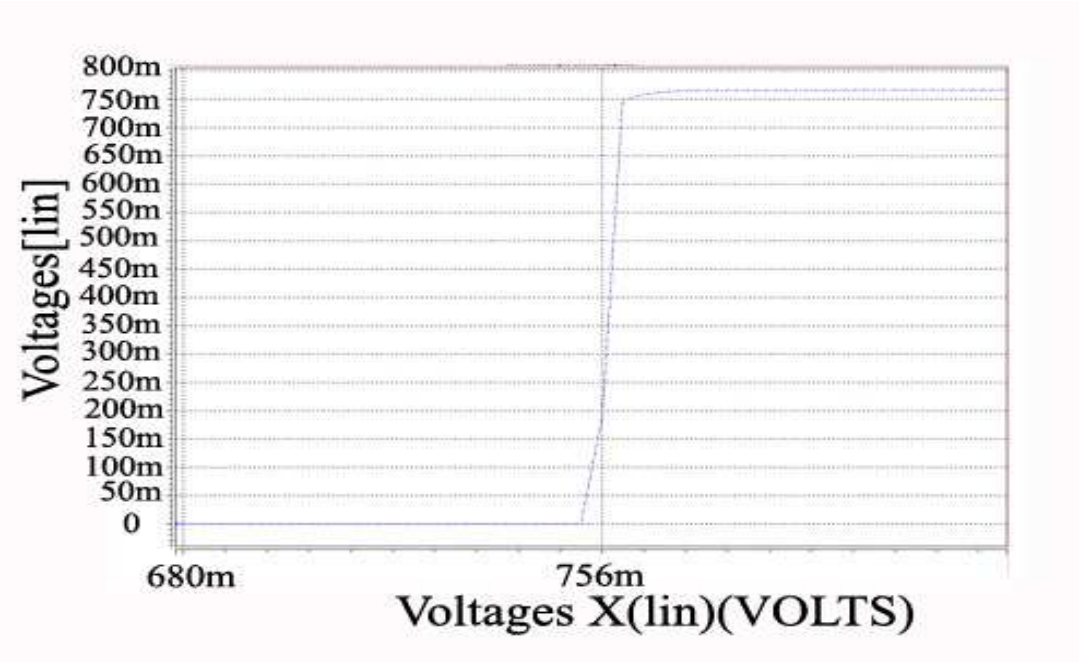


Fig. 5-14 Output Swing. (Appendix A.13)

4. PSRR

PSRR, Power-Supply Rejection Ratio. Assume that the chip ground is reliable. The test only on the supply. It turned out to be 125dB at 0dB.

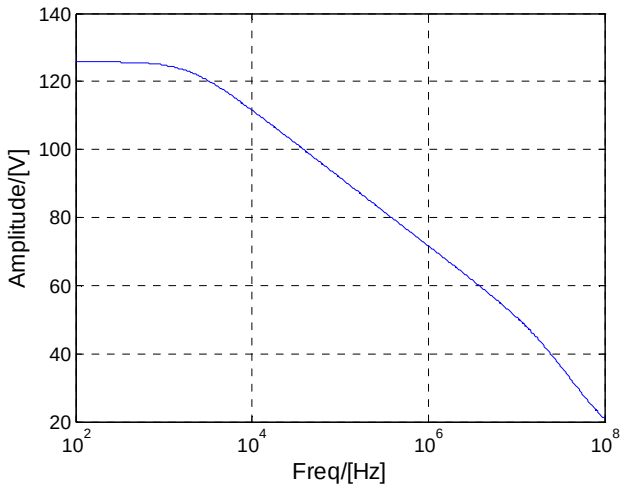


Fig. 5-15 PSRR Amplitude Frequency Response (Appendix A.15)

5. Settling Time

We added a tiny pulse on input. The Settling time is:

Settling Time+ = 31ns and Settling Time- = 73ns.

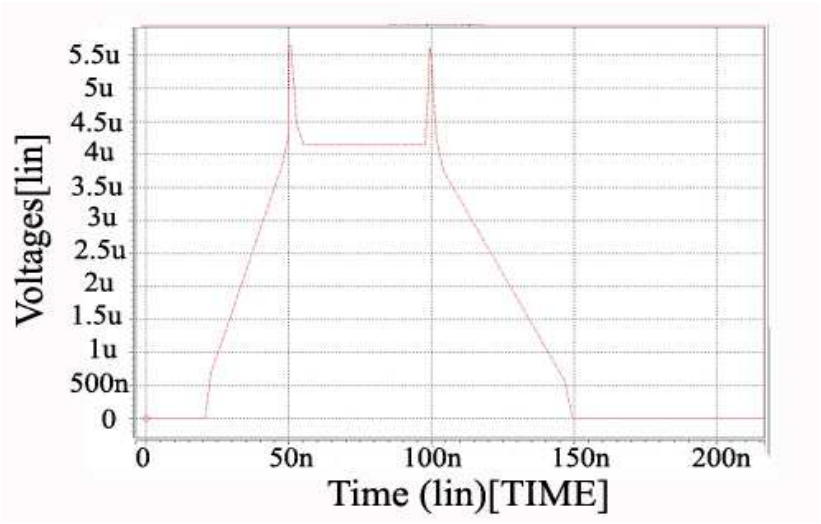


Fig16 Settling Time (Appendix A.15)

E. Summary

A low voltage single-supply operational amplifier for hearing aids application was designed in this paper. By using short channel devices, it works on a 1.3V single supply and get a gain of 82dB. The analog circuit involved in hearing aids design contributes a lot to the high performance of the chip. We will further our research on this area.

Spec	Designed Value	Simulation Value
Gain	80dB	82.47dB
Settling time +	--	31ns
Settling time -	--	73ns
ICMR +	710mV	710mV
ICMR -	690mV	690mV
CMMR	50dB	85dB
PSRR+	>60dB	125.7dB
Output Swing+	750mV	767V
Output Swing_	0V	0V
Output Resistance	As small as possible	12.3k
Input Resistance	Infinite	1.0e20
Total Power Dissipation	--	73.1μWatt

Table 5-6 Specifications of The Single-Supply Op-amp.

IV. Conclusion

Hearing aids specialized CMOS low-voltage, low-power operational amplifiers and analog building blocks are described in this thesis as well as the design methodologies with considering of submicron channel effects.

The application of short channel devices helps to get the conventional designs to meet the requirements of the circuit specifications. It results in the development of new design methods in the submicron scales.

In these thesis, I gave circuit description netlist files, simulation netlist files, optimization netlist files and amplifier testing configurations also. It may help readers to understand the HSPICE and the simulation tool. Equations were also given. The are of great importance for design engineers. A basic principle of analog integrated circuit design is that do not turn to simulation before you know the output. On front-end design there are many things to be discussed later, for example, the noise control, new low-power circuit configurations, new low-voltage circuit configurations and frequency domain analysis, etc. As an engineering research, a practical test, MPW is needed to test our design. That is another story totally different.

Finally, please allow me to give my gratefulness and best wish to my Korean friends. Many thanks to my respected advisor, professor Jarng. He gives me guidance on the research and the thesis. Many thanks to lab mates who are also my dear friends. It is them who helped me a lot on my study and life in Korea. They are, Mrs. Gwon, Dr. Lee, Kyong-sock, Jae-ha, Dae-jin, Yu-ri-ae, Kyung-huan, and many.

IIV. References

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VIII. Appendix

A. Spice Netlist

1. DC Transfer Characteristic

```
TITLEL: Samsung .18u op-amp, with 60db gain. Sub-circuit design.
* This program is for the test of DC transfer characteristic
VIN+ nvin+ 0 DC 1.4
VIN- nvin- 0 DC 2.0
VDD nvdd 0 DC 2
VSS 0 nvss DC 0
CL nvout 0 10P                          * Load capacitor
.param lm = .18u
x1 nvdd nvss nvout nvin- nvin+ opamp1                  * Subcircuit.
.subckt opamp1 4 9 6 2 1                               * Subcircuit. Define
M1 4 2 3 9 Mn1 W = 3.3020u  L = LM
 M2 5 1 3 9 mn1 W = 3.3020u          L = LM
 M3 4 4 8 8 mp1 W = 302.9460n    L = LM
 M4 5 4 8 8 mp1 W = 302.9460n    L = LM
 M5 3 7 9 9 mn1 W = 257.1072n    L = LM
 M6 6 5 8 8 mp1 W = 5.8743u      L = LM
 M7 6 7 9 9 mn1 W = 2.7555u      L = LM
 M8 7 7 9 9 mn1 W = 726.4849n    L = LM
 m9 7 7 8 8 mp1 W = 1.7579u      L = LM
 CC 6 5 3p
```

```
.ends opamp1
.lib '/usr/COMLIB/L18/PRE_RULE/SPICE/L18_bsim3.lib_r1.0d' nn
* From this Library, the HSPICE get transistor models.
.dc vin- 0 2.0 0.1                    * DC sweep of voltage source,
vin-.
.PRINT DC V(nvout)                    * Show the result.
.END
```

2. Open-Loop Gain and Frequency response

```
TITLEL: Samsung .18u opamp, with 60db gain. subcircuit design.
* This program is for the testing of frequency response.
VIN+ nvin+ 0 DC = 1.17 AC = 1m
VIN- 10 0 DC 1.17
VDD nvdd 0 DC 2
VSS 0 nvss DC 0
CL nvout 0 10P
ct nvin- 10 100e-9
rt nvin- nvout 5e10
.param lm = .18u
x1 nvdd nvss nvout nvin- nvin+ opamp1
.subckt opamp1 8 9 6 2 1
M1 4 2 3 9 Mn1 W = 3.3020u  L = LM
 M2 5 1 3 9 mn1 W = 3.3020u          L = LM
 M3 4 4 8 8 mp1 W = 302.9460n    L = LM
 M4 5 4 8 8 mp1 W = 302.9460n    L = LM
 M5 3 7 9 9 mn1 W = 257.1072n    L = LM
```

```
 M6 6 5 8 8 mp1 W = 5.8743u      L = LM
 M7 6 7 9 9 mn1 W = 2.7555u      L = LM
 M8 7 7 9 9 mn1 W = 726.4849n    L = LM
 m9 7 7 8 8 mp1 W = 1.7579u      L = LM
 CC 6 5 3p
.ends opamp1
.lib '/usr/COMLIB/L18/PRE_RULE/SPICE/L18_bsim3.lib_r1.0d' nn
.op
.ac dec 30 1 30meg                          * AC sweep, from 1Hz to 30 megHz
.PRINT AC V(nvout) VP(nvout) vdb(nvout,nvin+)      * There are three
output, output voltage, phase, and gain.
.END
```

3. Output Swing.

```
TITLEL: Samsung .18u opamp, with 60db gain. subcircuit design.
* This program is for the test of Output swing.
VIN+ nvin+ 0 DC 1.2
VIN- nvin- 0 DC 2.0
VDD nvdd 0 DC 2
VSS 0 nvss DC 0
CL nvout 0 10P
r2 nvin- 0 10k
r1 nvin- nvout 100k
.param lm = .18u
x1 nvdd nvss nvout nvin- nvin+ opamp1
```

```
.subckt opamp1 8 9 6 1 2
 M1 4 2 3 9 Mn1 W = 3.3020u          L = LM
 M2 5 1 3 9 mn1 W = 3.3020u          L = LM
 M3 4 4 8 8 mp1 W = 302.9460n    L = LM
 M4 5 4 8 8 mp1 W = 302.9460n    L = LM
 M5 3 7 9 9 mn1 W = 257.1072n    L = LM
 M6 6 5 8 8 mp1 W = 5.8743u      L = LM
 M7 6 7 9 9 mn1 W = 2.7555u      L = LM
 M8 7 7 9 9 mn1 W = 726.4849n    L = LM
 m9 7 7 8 8 mp1 W = 1.7579u      L = LM
 CC 6 5 3p
.ends opamp1
.lib '/usr/COMLIB/L18/PRE_RULE/SPICE/L18_bsim3.lib_r1.0d' nn
.op
.dc vin- 0 2.0 0.05
.PRINT dC V(nvout)
.END
```

The result.

4. Settling Time

```
TITLEL: Samsung .18u opamp, with 40db gain. subcircuit design.
* Testing the settling time.
VIN- nvin- 0 pwl (0 1.2 20n 1.2 21n 1.4 169n 1.4 170n 1.2 300n 1.2)    *        a
pulse
* Give a pluse. Use a short rising time and falling time. The pulse lasted for
140ns.
```

```
voi nvout nvin+ 0
VDD nvdd 0 DC 2
VSS 0 nvss DC 0
CL nvout 0 10P
.param lm = .18u
x1 nvdd nvss nvout nvin- nvin+ opamp1
.subckt opamp1 8 9 6 1 2
 M1 4 2 3 9 Mn1 W = 3.3020u L = LM
 M2 5 1 3 9 mn1 W = 3.3020u L = LM
 M3 4 4 8 8 mp1 W = 302.9460n    L = LM
 M4 5 4 8 8 mp1 W = 302.9460n    L = LM
 M5 3 7 9 9 mn1 W = 257.1072n    L = LM
 M6 6 5 8 8 mp1 W = 5.8743u      L = LM
 M7 6 7 9 9 mn1 W = 2.7555u      L = LM
 M8 7 7 9 9 mn1 W = 726.4849n    L = LM
 m9 7 7 8 8 mp1 W = 1.7579u      L = LM
 CC 6 5 3p
.ends opamp1
.lib '/usr/COMLIB/L18/PRE_RULE/SPICE/L18_bsim3.lib_r1.0d' nn
.op
.option nomod post
.tran .5n 300n
* Transient analysis. Because our desired value is about 10ns, the analysis
continues for 300ns.
.print tran v(nvout) v(nvin-)
.probe tran v(nvout) v(nvin-)
.END
```

5. Common-Mode Range (CMR)

```
TITLEL: Samsung .18u opamp, with 60db gain. subcircuit design.
* This program is for the testing of the Common-mode range
VIN- nvin- 0 DC 2.0
VDD nvdd 0 DC 2
VSS 0 nvss DC 0
CL nvout 0 10P
voi nvout nvin+ 0
.param lm = .18u
x1 nvdd nvss nvout nvin- nvin+ opamp1
.subckt opamp1 8 9 6 1 2
 M1 4 2 3 9 Mn1 W = 3.3020u          L = LM
 M2 5 1 3 9 mn1 W = 3.3020u          L = LM
 M3 4 4 8 8 mp1 W = 302.9460n    L = LM
 M4 5 4 8 8 mp1 W = 302.9460n    L = LM
 M5 3 7 9 9 mn1 W = 257.1072n    L = LM
 M6 6 5 8 8 mp1 W = 5.8743u      L = LM
 M7 6 7 9 9 mn1 W = 2.7555u      L = LM
 M8 7 7 9 9 mn1 W = 726.4849n    L = LM
 m9 7 7 8 8 mp1 W = 1.7579u      L = LM
 CC 6 5 3p
.ends opamp1
.lib '/usr/COMLIB/L18/PRE_RULE/SPICE/L18_bsim3.lib_r1.0d' nn
.op
.option nomod post
```

```
.dc vin- -2 4.0 0.05
.print dC V(nvout)
.PRobe dC V(nvout)
.END
```

7. Power Supply Rejection Ratio (PSRR)

Code for PSRR+:

```
TITLEL: Samsung .18u opamp, with 40db gain. subcircuit design.
* This program is for PSRR+ (Positive Power Supply Rejection Ratio)
VIN- nvin- 0 DC 1.17
VDD nvdd 0 DC 2 AC .1
VSS 0 nvss DC 0
vio nvin+ nvout ac = 0 dc = 0
CL nvout 0 10P
.param lm = .18u
x1 nvdd nvss nvout nvin- nvin+ opamp1
.subckt opamp1 8 9 6 2 1
 M1 4 2 3 9 Mn1 W = 3.3020u          L = LM
 M2 5 1 3 9 mn1 W = 3.3020u L = LM
 M3 4 4 8 8 mp1 W = 302.9460n    L = LM
 M4 5 4 8 8 mp1 W = 302.9460n    L = LM
 M5 3 7 9 9 mn1 W = 257.1072n    L = LM
 M6 6 5 8 8 mp1 W = 5.8743u      L = LM
 M7 6 7 9 9 mn1 W = 2.7555u      L = LM
 M8 7 7 9 9 mn1 W = 726.4849n    L = LM
 m9 7 7 8 8 mp1 W = 1.7579u      L = LM
```

```
 CC 6 5 3p
.ends opamp1
.lib '/usr/COMLIB/L18/PRE_RULE/SPICE/L18_bsim3.lib_r1.0d' nn
.op
.ac dec 10 1 100meg
.print ac pssr+ = par('20*log10(.1/v(nvout))') vp(nvout)
.end
```

Code for PSRR-:

```
TITLEL: Samsung .18u opamp, with 40db gain. subcircuit design.
* This program is for PSRR- (Positive Power Supply Rejection Ratio)
VIN+ nvin+ 0 DC 1.17
VDD nvdd 0 DC 2
VSS 0 nvss DC 0 AC .1
vio nvin- nvout ac = 0 dc = 0
CL nvout 0 10P
.param lm = .18u
x1 nvdd nvss nvout nvin- nvin+ opamp1
.subckt opamp1 8 9 6 2 1
 M1 4 2 3 9 Mn1 W = 3.3020u          L = LM
 M2 5 1 3 9 mn1 W = 3.3020u L = LM
 M3 4 4 8 8 mp1 W = 302.9460n    L = LM
 M4 5 4 8 8 mp1 W = 302.9460n    L = LM
 M5 3 7 9 9 mn1 W = 257.1072n    L = LM
 M6 6 5 8 8 mp1 W = 5.8743u      L = LM
 M7 6 7 9 9 mn1 W = 2.7555u      L = LM
 M8 7 7 9 9 mn1 W = 726.4849n    L = LM
```

```
 m9 7 7 8 8 mp1 W = 1.7579u       L = LM
 CC 6 5 3p
.ends opamp1
.lib '/usr/COMLIB/L18/PRE_RULE/SPICE/L18_bsim3.lib_r1.0d' nn
.op
.ac dec 10 1 100meg
.print ac pssr- = par('20*log10(.1/v(nvout))') vp(nvout)
.end
```

8 Differential Pair

```
****N channel differential pair*****
.lib '/usr/COMLIB/L18.lib' nn
.option post = 2

vdd 4 0 1.3
vinn 1 0 sin(.7 .01m 1000 0 0 )
vinp 2 0 .7
rref 7 8 10k

m1 3 1 5 5 nch w = 16u l = 1u
m2 6 2 5 5 nch w = 16u l = 1u
m3 3 3 4 4 pch w = 23.70u l = 1u
m4 6 3 4 4 pch w = 23.70u l = 1u
m5 5 7 0 0 nch w = 10.63u l = 1u
m6 7 7 0 0 nch w = 10.63u l = 1u
m7 8 8 4 4 pch w = 10u l = 1u
.op
```

```
.tf v(6) vinn
.tran .01m 5m
.print tran v(6)
.end
```

9_a Gain Stage

```
********** Gain stage **********
.lib '/usr/COMLIB/L18.lib' nn
.option post = 2
vdd 4 0 1.3
ib 10 0 25u
vin 1 0 sin( .75 .1m 1000 0 0)
.para lm = 1u
m8 9 10 4 4 pch w = 46.78u l = lm
m9 9 1 0 0 nch w =10.91u l = lm
*m10 11 11 0 0 nch
m11 10 10 4 4 pch w = 13.56u l = lm

.op
.tf v(9) vin
.tran .01m 5m
.print tran v(9)
.end
```

9_b Gain Stage

```
********** Gain stage **********
.lib '/usr/COMLIB/L18.lib' nn
```

```
.option post = 2
vdd 4 0 1.3
ib 10 0 25u
vin 1 0  sin( .75 .1m 1000 0 0)
.para lm = 1u
m8 9 10 4 4 pch w = 46.78u l = lm
m9 9 1 0 0 nch w =10.91u l = lm
*m10 11 11 0 0 nch
m11 10 10 4 4 pch w = 13.56u l = lm

.op
.tf v(9) vin
.ac dec 100 0 100x
.dc ac vdb(9) vp(9)
.end
```

10 Output Stage

```
**** N-channel Source Follower with Bias.****
.lib '/usr/COMLIB/L18.lib' nn
.option post = 2
 vdd 4 0 1.3
 vin 1 0 sin(.9 .1 1000 0 0)      * Input signal
* vin 1 0 dc = .7
 m1 4 1 2 2 nch w= .42u l = .18u
 m2 2 3 0 0 nch w= .22u l = .18u
 m3 3 3 0 0 nch w= .22u l = .18u
```

```
 m4 5 5 3 3 nch w= 2.0u l = 1u
 rref 4 5 10k
 rload 2 0 8k

 .tf v(2) vin                    * Small signal analysis
 .op
 .tran .01m 5m
 .print tran v(2)
* .dc vin 0 2 .1
* .print dc v(2)
 .end
```

11 Full Operational Amplifier

```
*** The Full operational amplifier ***********
.lib '/usr/COMLIB/L18.lib' nn
.option post = 2

vdd 4 0 1.3
*vinn 1 0 sin(.7 .01m 1000 0 0 )
vinn 2 0 dc = .7 ac = 0.01m
vinp 1 0 .7
rref1 7 8 10k
rref2 4 11 80k
rload 10 0 10k
m1 3 1 5 5 nch w = 16.00u l = 1u
m2 6 2 5 5 nch w = 16.00u l = 1u
```

```
m3 3 3 4 4 pch w = 23.70u l = 1u
m4 6 3 4 4 pch w = 23.70u l = 1u
m5 5 7 0 0 nch w = 10.63u l = 1u
m6 7 7 0 0 nch w = 10.63u l = 1u
m7 8 8 4 4 pch w = 10u l = 1u

m8 9 6 4 4 pch w = 47.31u l = 1u
m9 9 7 0 0 nch w = 10.63u l = 1u

 m10 4 9 10 10 nch w= .42u l = .18u
 m11 10 12 0 0 nch w= .22u l = .18u
 m12 11 11 12 12 nch w= .22u l = .18u
 m13 12 12 0 0 nch w= .22u l = .18u
.op
.tf v(10) vinn
.tran .01m 5m
.print tran v(10)
*.ac dec 100 0 100x
*.print ac vdb(10, 2) vp(10)
.meas tran p_sup avg power
.meas tran eff param='100*p_load/p_sup'
.end
```

B. Library Information

The libraries used in this thesis are:

1. Samsung 0.18um analog library
2. Dongbu-ANAM 0.18um mixed-signal library.