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Nine-Level Inverter Based on Switched-Capacitor Structure with Single Source

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Abstract : This paper discusses a new configuration of the switched-capacitor multilevel inverter (SCMI). Similar to conventional multilevel inverters, the features of the proposed SCMI are the same with the multilevel inverters but uses less number of active switches than the other multilevel inverters have the same number of levels output voltage. As a result, the cost and size of the system are reduced compared to the previous configurations. In the proposed topology, the capacitor voltage can be self-balance without using any auxiliary circuit. By using the capacitor, the output voltage is stepped up from the input voltage and without employing transformer. To verify the operation principle, PSIM simulation is performed for 9-level configuration. The experimental results are also shown with 9-level inverter configuration.

Keyword : Multilevel inverter, switched capacitor, single-phase inverter, PWM control.

1. Introduction

Recently multi-level inverter technologies have become more attractive for researchers and manufacturers because they have some advantages over the conventional three-level pulse width modulation (PWM) inverters. The multilevel inverter has the following advantages as improved output waveform quality, lower electromagnetic interference (EMI) and lower device stress [1]-[7]. Multi-level inverters include semiconductor switches capacitors, diodes, and supplies. When the switches are switching to supply the capacitor voltages, which increases the step-up gain ratio of the output voltage, while the voltage stress on the power semiconductors are reduced significantly. The multi-level inverter configuration is commonly used as neutral point clamped (NPC); capacitor-clamped (flying capacitors); and cascaded H-bridge inverter with separate dc sources. The most attractive features of multi-level inverters are that they improved output waveforms with lower THD, and they can operate with a lower switching frequency and smaller filter size and lower EMI.

The switched-capacitor (SC) nine-level inverter with a single dc source was presented in [8] with using a large number of switch. A combination of SC cells for SC multilevel inverters was proposed [9]. Each SC cell contains one diode, one capacitor and two switches. These topologies can boost voltage without the inductor. Moreover, the capacitor voltage in these topologies can be self- balance. The amount of the components in the circuit is lower than that in the traditional multi level inverters, it is still high though. The SC structure is added to the MI to boost voltage [10]-[13]. The switched-capacitor multi level inverter(SCMI) uses charging and discharging characteristics of the capacitor to reduce the number of the source in the circuit. The SCMI can be self-balance by switching the capacitors in parallel and in series through the switches. In the parallel mode, the capacitors are charged directly by power supply, while they release store energy during the series mode. By using SC structures, the system does not need more power supplies to increase the output voltage level or the transformers to boost output voltage. In the SCMI, the H-bridge circuit is generally used to change the state of the output voltage.

This paper presents a novel SCMI configuration which is combined with the H-bridge circuit to create output ladder voltage waveform in reducing the number of

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switches. The proposed SCMI does not use any inductors. This paper develops the theoretical operation of the proposed SCMI and verifies the operating principle through the simulation result of nine-level configuration by P.SIM 9.0 software. The study results are also demonstrated through experiments with inverter 9-level.

2. Proposed Topology

Fig.1 shows a proposed SC nine-level inverter topology. The proposed SCMI consists of two SC cells connected in parallel to the H-bridge circuit. The first SC cell is a combination of one capacitor, one diode and two switches (C_1-D_1-S_{11}-S_{12}), while the second SC cell includes one capacitor, one diode and three switches (C_2-D_2-S_{21}-S_{22}-S_{23}).

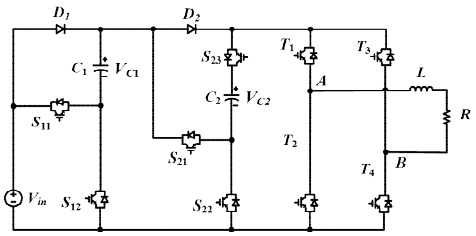
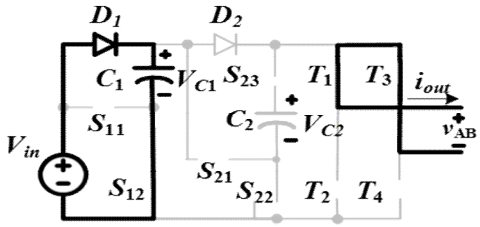


Figure 1. Proposed SC nine-level inverter topology.

In the operation circuit, the C_1 capacitor is charged in parallel connection with the input source through S_{12}, while it is discharged in series connection with the input source through S_{11}. Also, the C_2 capacitor is charged in parallel connection with the C_1 capacitor, input source through S_{22} and anti-parallel diode of S_{23}, while it is discharged in series connection with the C_1 capacitor and input source through S_{21},S_{23}.



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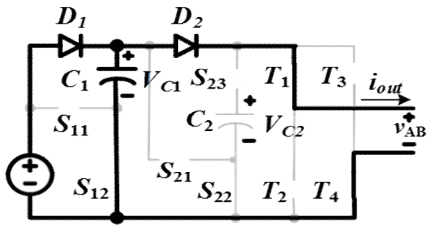

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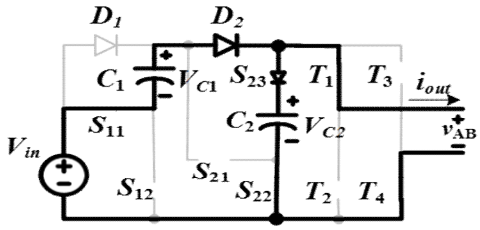


(c)

Figure 2. Operation states and current flow of proposed SCMI.
(a) state 1; (b) state 2; (c) state 3.

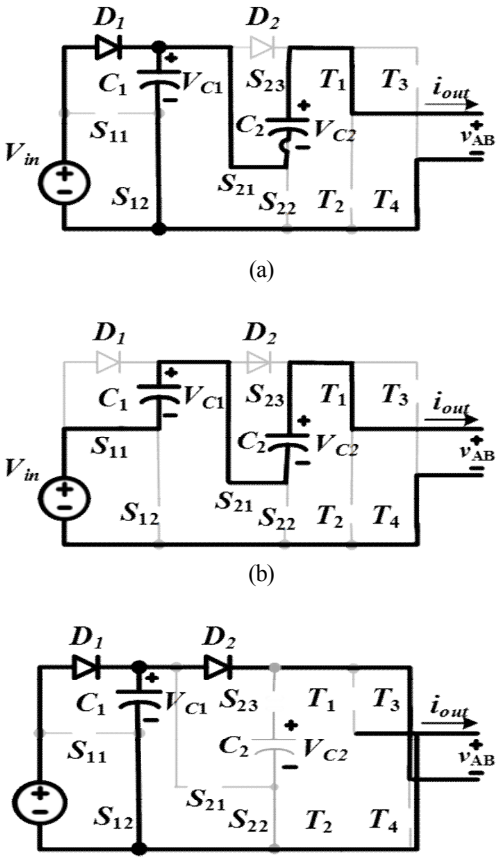
Figs. 2 and 3 show the operating states of the proposed SCMI. In the positive period, the circuit operation includes seven stages and four states [state 2 to state 5, Fig. 2(b), Fig. 2(c), Fig. 3(a), and Fig. 3(b)]. In this period, the switches of the H-bridged is not changed, T_1 and T_4 arefully turned ON, while T_2 and T_3 are fully turned OFF, the components of the SC cells are changed in each stage.

Stage 1 – [Fig. 2(a) and Fig. 2(b)]: S_{12}, S_{22} and T_1 are fully turned ON, while S_{11},S_{21},S_{23} and T_2 are fully turned OFF. The D_1 diode is forward-biased. The C_1 capacitor is charged from the input voltage, and $VC_1=V_{in}$. If T_3 is turned ON and T_4 is turned OFF, the output voltage is zero($V_{AB}= 0$) as shown in Fig. 3(a) for state 1. If T_3 is turned OFF and T_4 is turned ON, the output voltage is the input voltage($V_{AB}= V_{in}$) as shown in Fig. 3(b) for state 2.

Stage 2 – [Fig. 2(b) and Fig. 2(c)]: S_{22} is fully turned ON, while S_{21} and S_{23} are fully turned OFF. The D_2 diode is forward-biased. If S11 is turned OFF and S_{12} is turned ON, the D_1 diode is forward-biased, the C_1 capacitor is charged from input voltage. The output voltage is $V_{AB}=V_{C2}=V_{in}$ as shown in Fig. 2(b) for state 2. If S_{11} is turned ON and S_{12} is turned OFF, the D_1 diode is reverse-biased, the C_1 capacitor is discharged while the C_2 capacitor is charged from input voltage and C_1 capacitor voltage, and $V_{C2}=V_{in}+V_{C1}=2V_{in}$. The output voltage equals twice the input voltage ($V_{AB}=V_{C2}=2V_{in}$) as shown in Fig. 2 (c) for state 3.

Stage 3 – [Fig. 2(c) and Fig. 3(a)]: If S11 and S_{22} are turned ON and S_{12}, S_{21} and S_{23} are turned OFF, the D_1 diode is reverse-biased, the D_2 diode is forward-biased, the C_1 capacitor is discharged, while the C_2 capacitor is charged from input voltage and C_1 capacitor voltage. The output voltage is VAB= $V_{in}+V_{C1}=2V_{in}$ as shown in Fig.3.2(c) for state 3. If S_{11} and S_{22} are turned OFF and S_{12}, S_{21} and S_{23} are turned ON, the D_1 diode is forward-biased, the D_2 diode is reverse-biased, the C_1 capacitor is charged from input voltage, while the C_2 capacitor is discharged, and the output voltage equals three times of the input voltage

(V_{AB}= V_{in}+V_{C2}=3V_{in}) as shown in Fig. 3(a) for state 4.



(a)

(b)

(c)

Figure 3. Operation states and current flow of proposed SCMI.
(a) state 4; (b) state 5; (c) state 6.

Stage 4 - [Fig. 3(a) and Fig. 3(b)]: S_{21} and S_{23} are fully turned ON, while S_{22} is fully turned OFF. The D_2 diode is reverse-biased, and the C_2 capacitor is discharged. If S_{12} is turned ON and S_{11} is turned OFF, the D_1 diode is forward-biased, the C_1 capacitor is charged from input voltage. The output voltage is V_{AB}=V_{in}+V_{C2}=3V_{in} as shown in Fig. 3(a) for state 4. If S_{12} is turned OFF and S_{11} is turned ON, the D_1 diode is reverse-biased, the C_1 capacitor is discharged ; and the output voltage equals four times of the input voltage (V_{AB}=V_{in}+V_{C1}+V_{C2}=4V_{in}) as shown in Fig. 3(b) for state 5.

Stage 5 - [Fig. 2(c) and Fig. 3(a)]: similar to the stage 3.

Stage 6 - [Fig. 2(b) and Fig. 2(c)]: similar to the stage 2.

Stage 7 - [Fig. 2(a) and Fig. 2(b)]: similar to the stage 1.

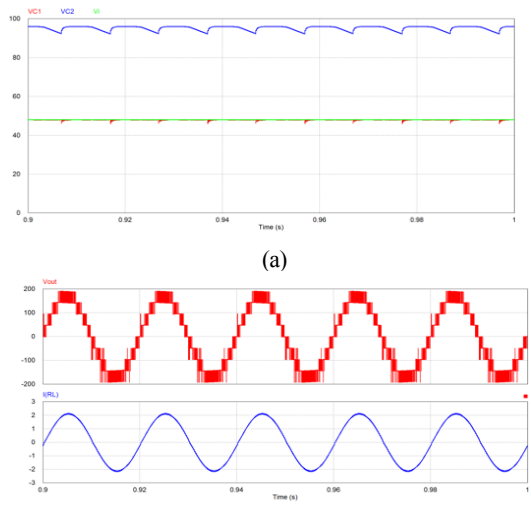
3. Results

To confirm the operation of the proposed SCMI, the simulation was performed for the proposed SCMI. The parameters of the proposed topology are chosen as listed in Table I. Simulations were tested for the inductive load (R=80Ω, L=30mH). The proposed SCMI produces 50-Hz sinusoidal voltage waveform with the desires output voltage of 122 VRMS. The simulation was worked by PSIM 9.1 with the parameters is in Table1.

Table 1. Parameters for Simulation and Experiment

Input voltage (V_{in})	48 V
Output voltage in RMS (V_{AB})	120 V
Capacitors (C_1 = C_2)	2200 μF
Carrier frequency (f_{car})	5 kHz
Output frequency (f_{ref})	50 Hz

Fig. 4 shows the simulation results with M=3.6, the inductive load (R=80Ω and L=30mH). The capacitors C_1 and C_2 voltage are 47.5V and 95V. The ripple voltage of the capacitors C_1 and C_2 are 1.5V and 3.5V, respectively. The load current lags the output voltage, the output and current voltage waveforms are shown in the Fig. 4(b). The output current waveform is shown in the Fig. 4(b) with the maximum current of 2.2 A.



(a)

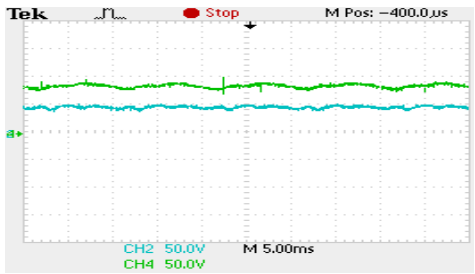
(b)

Figure 4. Simulation results with M = 3.6, inductive load R = 80 Ω and Lo = 30 mH. From top to bottom:
(a) input voltage, capacitors C_1 and C_2 voltage;
(b) output voltage waveform (V_o) with the resistive load.

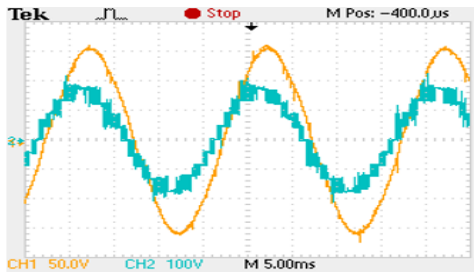
Based on the simulation results, the prototype of experiment was performed with the parameters as in the Table 1. Fig.5 shows the experimental results with the inductive load. Fig.5(a) shows the voltage waveform of the C_1 and C_1 capacitors. The maximum and minimum capacitor C_1 voltages are 48V and 41V, respectively. So, the ripple voltage of C_1 is 7V. The maximum and minimum capacitor C_2 voltages are 96V and 83.7V, respectively. So, the ripple voltage of C_2 is 12.3V. Fig.5(b) shows the output voltage waveform with nine-level. The total harmonic distortion (THD) of the output voltage and load R voltage are measured 2.8% and 10.7 % as shown in Fig.5(c) and Fig.5(d), respectively. The output voltage is 120 V_{RMS} with the frequency of 50Hz. And output current is 1.5A_{RMS} with the frequency of 50Hz.

4. Conclusion

A new switched-capacitor multilevel inverter (SCMI) topology has been proposed. The proposed SCMI has a lower number of components than the traditional MIs. By switching the capacitor in series and in parallel, the output voltage is larger than the input voltage with self-balanced capacitors. Operating principle and circuit analysis of the proposed SC nine-level inverter were shown. In order to verify the performance of the proposed converter, the laboratory prototype based on TMS320F2812 DSP and PSIM simulation have been performed. The simulation and the experimental results match to theory.



(a)



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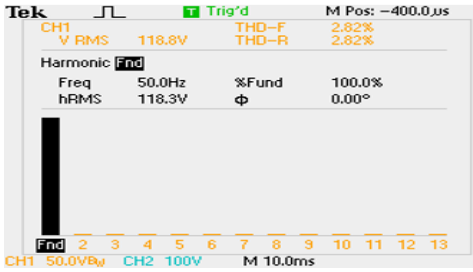

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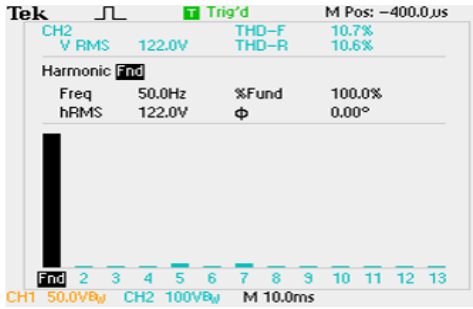

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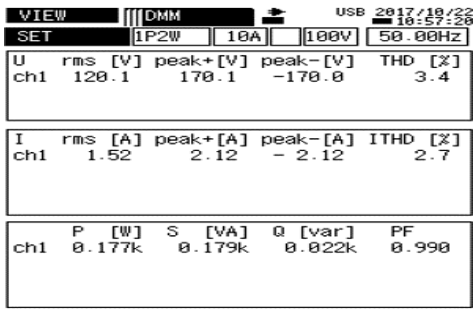

(e)

Figure 5. Experimental results with inductive load
(R = 80 Ω, L = 30 mH)
(a) Capacitors C1 and C_2 voltage
(b)Output voltage waveforms(V_{AB} and V_R)
(c)-(d)harmonics of voltage waveform on resistor and output voltage and the outputpower.

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