August 2019
Master's Degree Thesis

A 10-bit 500KS/s Low-Power Successive Approximation Register Analog-to-Digital Converter for Implantable Bio-medical Device Application

Graduate School of Chosun University

Department of Information and Communication

Engineering

Unse Fatima

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체내 삽입 생-의학장치 응용을 위한 10비트 500KS/s 저전력 SAR 아날로그-디지털 변환기

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Advisor: Prof. Choi Goang-Seog

A thesis submitted in partial fulfillment of the requirements for a master's degree

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석사학위논문을 인준함

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Acronyms

ADC	Analog to digital converter
AFE	Analog-Frontend
DAC	Digital-to-Analog Converter
DNL	Differential Non Linearity
DSP	Digital Signal Processing
ENOB	Effective Number of Bits
IC	Integrated Circuit
I/O	Input/output
INL	Integral Non Linearity
LSB	Least Significant Bit
MIM	Metal Insulator Metal
MSB	Most Significant Bit
OSR	Over-Sampling Ratio
RMS	Root Mean Square
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
S/H	Sample and Hold
SINAD	Signal-To-Noise and Distortion
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion

Abstract

A 10-bit 500KS/s Low-Power Successive Approximation Register Analog-to-Digital Converter for Implantable Bio-medical Device Application

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As biomedical implant devices are becoming more prevalent, requirement to modify their power, performance and ergonomics contemporaneously is also increasing. This thesis presents a 10-bit 500kS/s successive approximation register (SAR) ADC operating at ultra-low power for biomedical implant devices. A binary weighted split capacitor digital to analog converter architecture and a half scaled reference voltage based monotonic switching scheme is implemented to reduce total capacitor count, area and power consumption. An ultra-low power consuming dynamic comparator with body biasing technique is employed in contemplation of complying with power limitations of implantable biomedical devices. This work is presented using a 180-nm CMOS process. The measurement results exhibit that the ADC

achieves 8.57 ENOB at 1.8 V supply voltage with a SNDR of 55.8 dB and SFDR of 63.4dB consuming 3.6-μW at a sampling frequency of 500 kS/s.

한글요약

체내 삽입 생-의학장치 응용을 위한 10비트 500KS/s 저전력 SAR 아날로그-디지털 변환기

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생물의학 임플란트 장치가 보편화됨에 따라, 동시대적으로 그 힘, 성능, 인체공학을 수정해야 하는 요건도 증가하고 있다. 본 논문은 생물의학 임플란트 장치에 대해 초저전력 작동으로 작동하는 10 비트 500kS/s SAR ADC 를 제시한다. 총 캐패시터 수, 면적 및 전력 소비량을 줄이기 위해 2 진 가중 분할 캐패시터 DAC 아키텍처와 1/2 스케일 기준 전압 단조 스위칭 방식을 구현한다. 인체 바이어싱 기법을 사용한 초저전력 소비 동적 비교기는 이식 가능한 생물의학 기기의 전력 제한 준수를 고려하는 데 사용된다. 이 작업은 180nm

CMOS 공정을 사용하여 완료된다. 측정 결과는 ADC 가 55.8dB 의 SNDR 로 1.8V 공급 전압에서 8.57 ENOB 를 달성하고, 500kS/s 의 샘플링 주파수에서 3.6μW 를 소비하는 63.4dB 의 SFDR 을 달성한다는 것을 보여준다.

Chapter 1: Introduction

1.1 Motivation

A variety of biomedical implanted devices and wearable sensors are envisaged to contribute significantly for preventive-oriented health maintenance in future. Over the past few years, improvisation in circuit design techniques and development in nanoscale technology resulted in better processing capabilities. Moreover, using right technical approach with advanced processing capabilities of integrated circuit (IC) technology leads to low power level systems which allow intricate biomedical operations to be entirely replaced by implanted devices. IC's processing capabilities are virtually infinite but in biomedical devices, energy is a highly restrained factor. Block diagram of general biomedical device is depicted in Figure 1. The fundamental modules of such device consists of communication, signal processing, data conversion and power management and uses sensing module to connect with biomedical environment. Without straining lifestyle of a carrier, a sophisticated biomedical device system must be developed. Applications of biomedical devices are shown in Figure 2. Recently, requirement for ultra-low power circuits for bio-signal procurement has been highly unprecedented. Analog to digital converter (ADC) is a key module which acts as an interface between analog-frontend (AFE) and digital signal processing (DSP) module in a biomedical devices. Therefore, an energy efficient ADC with specific design techniques must be employed to comply with the stringent of energy restraint [1]-[3]. As design of an ADC for a biomedical implant device is always being influenced by the stringent of

energy restraint in domains of architecture and implementation, therefore, power consumption and area are essential considerations in its design.

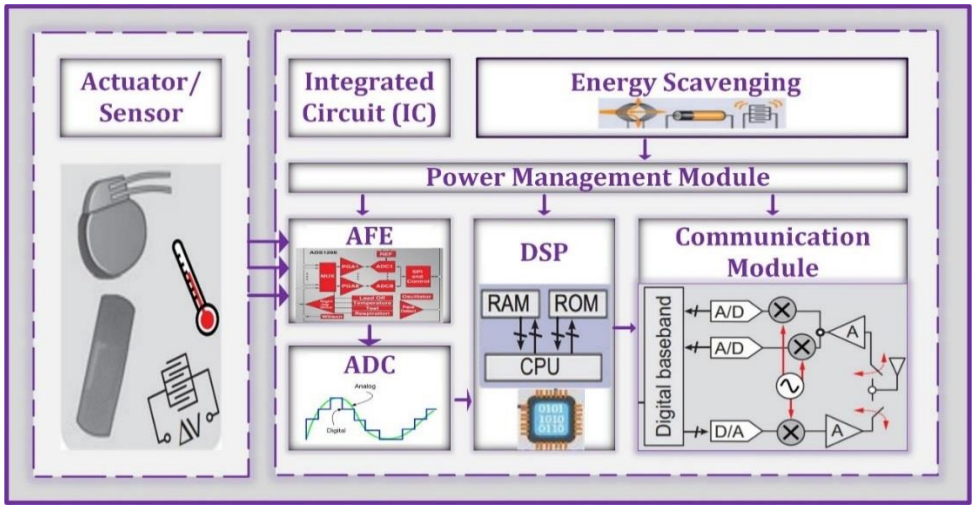


Figure 1. Generic Biomedical Device

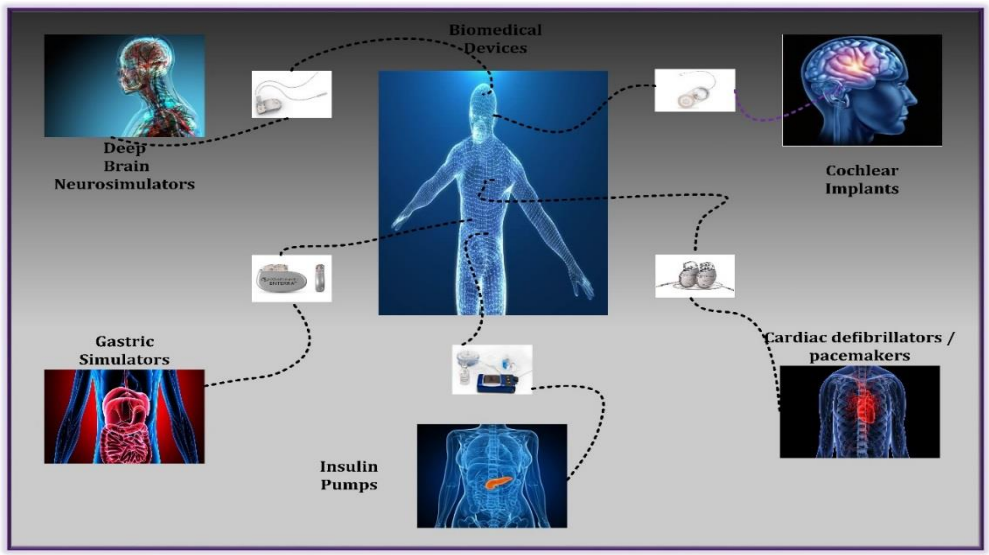


Figure 2. Applications of Biomedical Devices.

Among ADCs, the one that can leverage advanced processing capabilities with ultra-low power consumption, SAR ADC is the most suitable candidate [4]-[8].

1.2 Objectives

The foremost goal of this research is to learn the state-of-art methods used in a low power biomedical implanted devices SAR ADCs. I also aim to evaluate low power consumption characteristics of SAR ADC by using design techniques that can increase the overall performance and resolution of SAR ADC for biomedical implant devices using minimum analog circuitry, consuming less power.

1.3 Contributions

In this thesis, a SAR ADC addressing power constraints of biomedical devices has been presented. First, a binary weighted DAC with split capacitor is implemented with a monotonic switching scheme based on half scaled reference voltage to reduce area and hence power consumption. Secondly, a two stage dynamic comparator with a body biasing topology has been implemented, consuming very low power. And lastly SAR logic has been presented consisting of D-flip-flops. The major contributions of my work are as follows:

1. The implemented switching scheme in capacitive DAC array is achieved in two stages. In the first phase, most significant bit (MSB) is determined by using shifting level technique. In the second phase, half scaled reference based monotonic switching is used for least

significant bits (LSBs). By using this scheme, number of capacitors and switching energy is reduced considerably.

2. A two-stage dynamic comparator is employed in this ADC. It consists of a preamplifier and a latch stage. To undergo an ultra-low voltage operation along with improving dynamic offset, a reliable method of inserting a biased CMOS along with the body biasing topology is used.
3. Digital control circuitry comprising of successive approximation registers (shift register and latches), control logics and a clock generator has been used. As sampling rate is low, therefore static logic is used to avoid charge leakage.

1.4 Thesis Layout

This thesis is arranged as follows. Chapter 2 introduces various ADCs topologies each with its block diagram and performance metrics of ADCs. Chapter 3 analyzes different architectures of SAR ADC. Chapter 4 presents the circuit design of proposed SAR ADC for biomedical implant devices. Chapter 5 analyzes the simulation results of the implemented SAR ADC and conclusion is discussed in chapter 6.

Chapter 2: Literature Review

2.1 Topologies of ADC

ADCs have various topologies. The most famous ADC topologies include:

- Flash
- Folding & Interpolation
- Successive approximation register (SAR)
- Pipeline
- Sigma-delta

Each one has its own pros and cons. For example, the ADC which is appropriate for low resolution and high sampling rate application is flash ADC, while the ADC appropriate for a high resolution and low speed application is sigma delta ADC. So among all different types of ADCs, objective is to choose an ADC which is appropriate for our task and application. Above mentioned ADCs are described below briefly.

2.1.1 Flash ADC

The flash ADC:

- Matches the analog input by the reference threshold values.
- To obtain output as thermometer codes, the comparators compare the analog input by the reference voltages.

- These codes are then converted into the digital output. Generally, 2^N-1 comparators are necessary (N = output bits).
- A low resolution 4-bit flash ADC in [9] just consumes115 μW power at a sampling rate of 50 MSps.
- Flash topology is a worthy contender for low resolution high-speed applications. But, in this thesis, a resolution of 10-bit is required which means it would require $2^{10}-1$ comparators to build a 10-bit flash which is not feasible, as it will consume a lot of power.
- Figure 3 shows the modules which are used to construct a flash ADC.

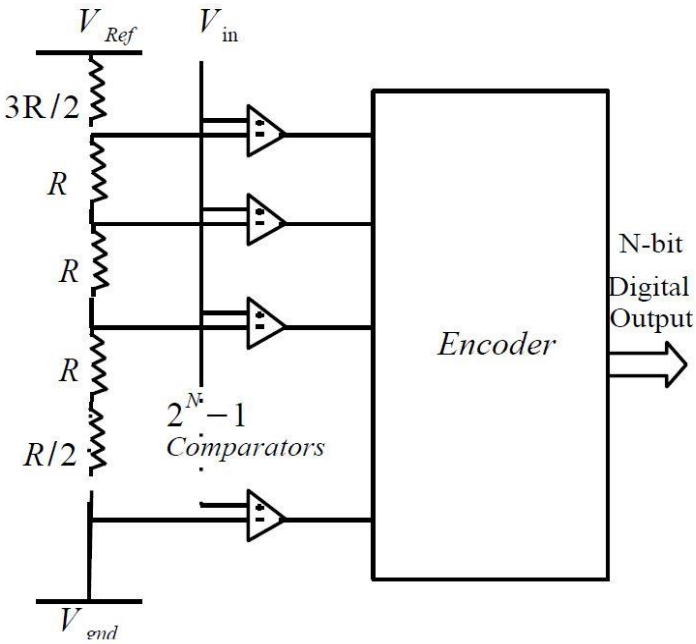
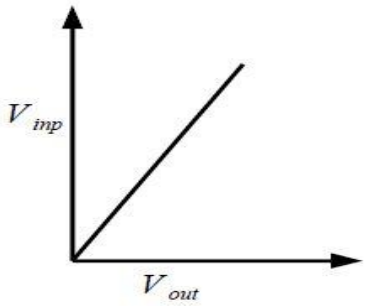


Figure 3. Block diagram of a flash A/D converter.

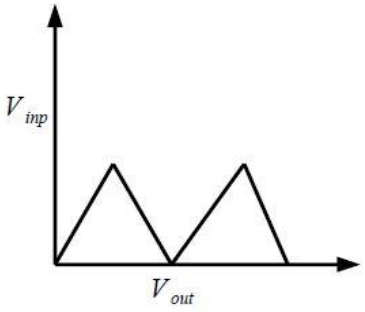
2.1.2 Folding and interpolating ADC

In this ADC:

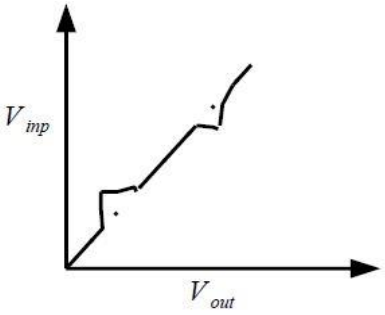
- The folder fundamentally folds the traditional linear I/O response to be inserted in between a smaller voltage range to reduce number of comparators.
- The diverse input and output graphs of a folding and interpolating A/D converter are presented in Figure 4.



(a) Unfolded Input & Output



(b) Single folded Input & Output



(c) Discontinuities on folded regions

Figure 4. Input & Output graphs of a folding and interpolating ADC.

- Double folding technique with other approaches (interpolation, averaging) are used to avoid the discontinuities in the output which occur because the CMOS transistors are incapable to give the requisite sharp folds.
- [10] gives us an insight of a 5 bit 2.2 mW and 1.75 Gsps ADC which makes use of unconventional techniques. Essentially, this type of design would suit a mediocre resolution of 4 to 8 bits at a sampling frequency which has a range above 100 MHz.
- This architecture inhabits more area as extra clocking circuitry is required by the interpolation and averaging methods.
- The requirement for the ADC in this project has a sampling rate below 1 MSps.

2.1.3 Successive approximation register (SAR) ADC

The SAR ADC:

- Uses a binary search algorithm to convert signal.
- Advantages:
  - It uses less analog modules in its design making its more compact.
  - It has a very low latency.
- Figure 5 demonstrates the block diagram of a SAR ADC.
- The SAR ADC consumes very less power. Latest SAR ADC designs [11]-[14] provide deep understandings into current trends.
- In a SAR ADC, all the modules have to operate at a frequency $N \times f s$.

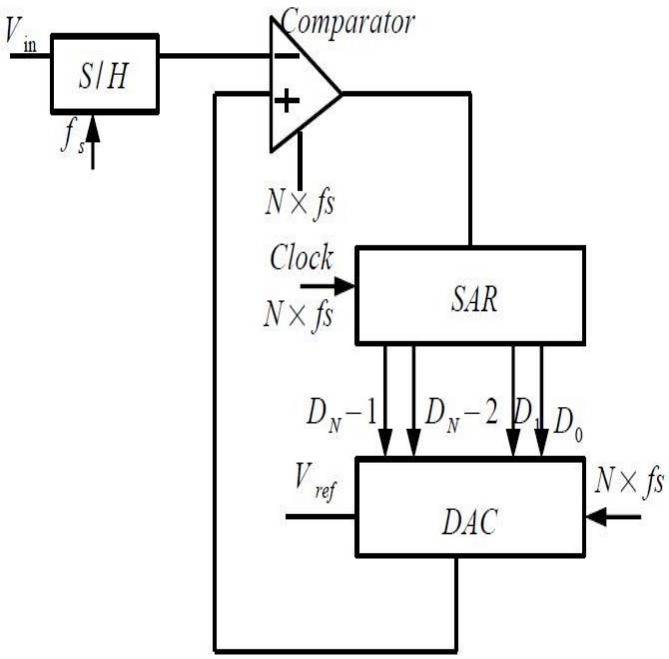


Figure 5. Block diagram of a SAR ADC.

2.1.4 Pipeline ADC

A pipeline ADC:

- Is an amplitude interleaving structure which constitutes of a stack of separate stages.
- Has each stage produces digital bits and residues.
- Has the residue streams from the stack until the finer bits gets resolved.
- Figure 6 depicts a pipeline architecture. This topology is appropriate for medium to high sampling rates [15]-[19].

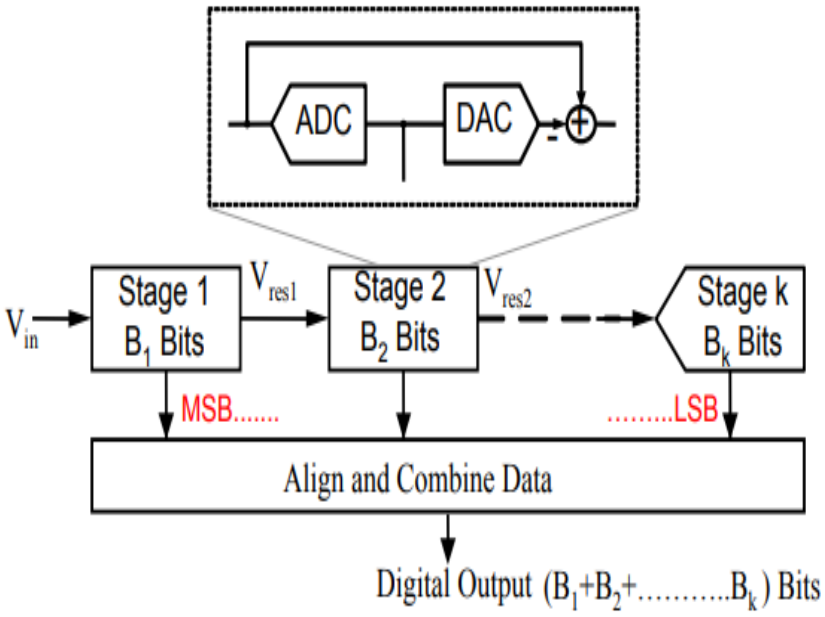


Figure 6. Block diagram of a pipeline ADC.

2.1.5 Sigma-delta converters (Σ/Δ)

Sigma Delta ADCs:

- Use pulse density modulation method.
- Are appropriate for the structures that involve high resolution and low sampling frequencies.
- Have a trade-off between sampling rate and resolution.
- The sigma-delta architecture uses feedback from the digital to the analog realm and requires a high OSR (10-128).
- Figure 7 is a sigma-delta block representation.

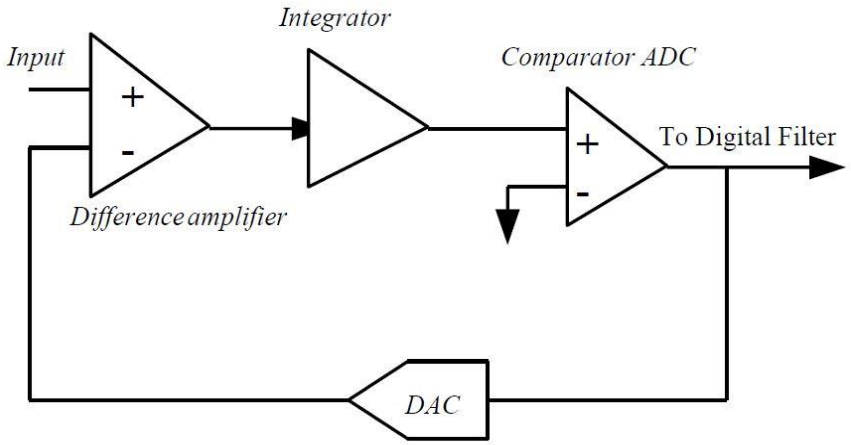


Figure 7. Block diagram of a sigma-delta ADC.

2.2 Analyzation of Topologies

After evaluating the ADC developments of the numerous topologies [20] a graph can be drawn as shown in Figure 8.

It can be perceived that:

- Sigma-delta ADC is appropriate for low speed and high-resolution applications.
- Pipeline ADC is suitable for moderate range of resolution and a mediocre sampling speed.
- Flash ADC would be a better choice for high speed low resolution applications.
- SAR ADC consumes very less power and has a medium range and resolution.
- Finally, for biomedical implantable devices' specifications on sampling rate, resolution and power consumption, SAR architecture would be the most appropriate choice.

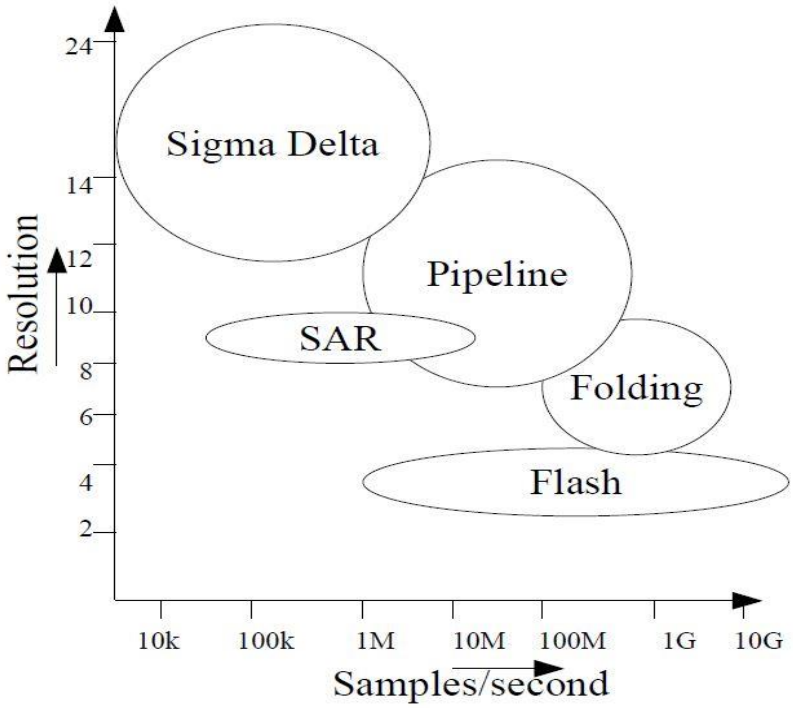


Figure 8. Sampling rate vs. resolution on various topologies.

2.3 ADC Performance Metrics

The term performance metrics refers to the criteria used in calculating errors associated with the structure. For instance, the criteria used to calculate how resistant an ADC is to noise is a dynamic one known as SNR while the static one used to measure the accuracy of the ADC is called as integral non linearity (INL), while SNR is a performance criterion used to measure how resistant the ADC is to noise.

2.3.1 DNL (Differential non linearity)

Differential non linearity is a criteria which is used to illustrate how far the present output code is away from an adjacent code. It is a comparison of actual output step signal with that of the ideal step signal. If the aforementioned difference exceeds 1 LSB, then this shows that missing codes are present in the output of ADC. Figure 9 shows the ideal transfer curve for a 2-bit ADC. This graph shows the input and the output of the ADC. Ramp signal characterizes the input signal by the dashed line while the output is denoted by the step signal.

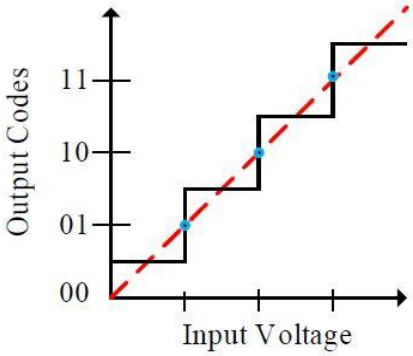


Figure 9. 2-bit ADC ideal transfer characteristic.

From the figure it can be seen that a step signal with equal step widths is considered as an ideal output. Whereas in a system where output is not ideal, these step widths are not equal as well. This difference between the widths of an ideal step and the actual step of the ADC is called as the DNL. A system exhibiting an unequal step width is shown in Figure 10. It demonstrates the variance amongst the ideal and the non-ideal widths.

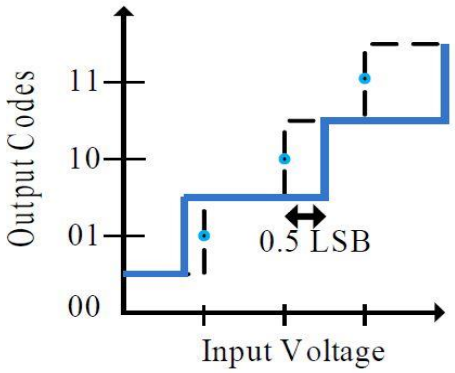


Figure 10. Deviation from the ideal transfer characteristic due to DNL.

2.3.2 INL (Integral non linearity)

The integral non-linearity (INL) is the deviancy of the ADC output as compared to its ideal transfer function. It is measured by calculating the magnitude at all code alterations and equating them with the magnitudes for ideal alterations.

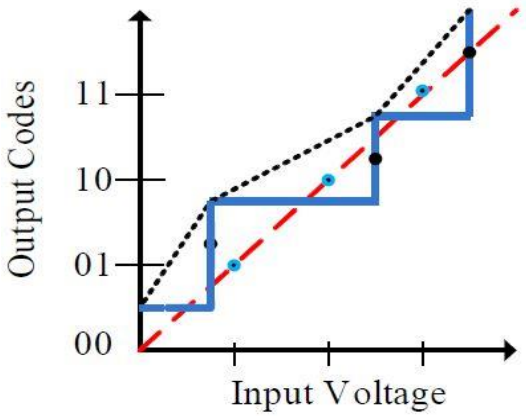


Figure 11. The INL deviation from ideal straight line.

The alteration amongst the ideal and the actual output voltage magnitude is known as the integral non-linearity error. Basically, INL error represents the sum of all DNL errors of the preceding ADC codes. In case of an ideal ADC, INL would be +0.5 LSB and -0.5 LSB. Figure 11 shows the INL error in which there is deviation from the ideal straight-line. Dashed line represents the ideal response whereas dotted line represents the actual response which is because of the INL. The INL is one of the most significant performance criteria for measuring the accuracy of an ADC.

2.3.3 Signal to noise ratio (SNR)

Signal to noise ratio is defined as the ratio of power of input signal to power of power (root mean square (RMS) value of signal and noise power are taken) Following equation describes it as:

$$\mathrm{SNR}_{(\mathrm{dB})} = 20\log\frac{\mathrm{V}_{\mathrm{signal}}}{\mathrm{V}_{\mathrm{noise}}} \qquad (1)$$

If *Vamp* is the maximum amplitude of a random input signal ranges from $0-V_{amp}$, then its root mean square power will be taken as V_{amp} $/2.2^{1/2}$. Considering the quantization noise power as V_{LSB} $/12^{1/2}$ generally. Putting them in (1) gives,

$$\mathrm{SNR}_{(\mathrm{dB})} = 20\log\frac{\frac{\mathrm{V}_{\mathrm{amp}}}{2\sqrt{2}}}{\frac{\mathrm{V}_{\mathrm{LSB}}}{\sqrt{12}}} \qquad (2)$$

$$\mathrm{SNR}_{(\mathrm{dB})} = 20\log\frac{3}{\sqrt{2}}\,2^{\mathrm{N}} \qquad (3)$$

$$\mathrm{SNR}_{(\mathrm{dB})} = 6.02\mathrm{N} + 1.76\mathrm{dB} \qquad (4)$$

Given that *N* is the resolution of ADC. Equation (4) gives the SNR for an ideal ADC. In reality ADC suffers from many different types of noise sources apart from quantization noise. Therefore in the reality, ADC has a SNR is not equal to that of in the equation (4) rather its less than this.

2.3.4 Spurious free dynamic range (SFDR)

Spurious free dynamic range which is also known as SFDR is described as the ratio of the output signal and the highest distortion (spur). A harmonic of the input signal frequency is generally called as spur.

2.3.5 Effective Number of Bits (ENOB)

ENOB is also called as the effective number of bits or effective bits. The resolution of ADC describes the total number of bits the ADC will have at its output, on the other hand ENOB tells how precise the ADC is, as it measures the complete accurateness of the ADC. It is given by

$$\mathrm{ENOB} = \frac{\mathrm{SINAD} - 1.76}{6.02} \tag{5}$$

However signal-to-noise and distortion (SINAD) can also be called as signal to-noise and distortion ratio (SNDR). SINAD is an amalgamation of the SNR and the total harmonic distortion (THD). As ENOB describes the whole ADC accurateness, it is one of the most significant dynamic performance metrics.

Chapter 3: SAR ADC Architecture

SAR ADC constitutes of four building blocks: a sample and hold circuit, a capacitor DAC, a dynamic latch comparator and a SAR logic circuit. Sampling process of analog input voltage is done by the sample and hold circuit depending upon architecture type. An analog voltage value is generated by DAC block which is compared with the sampled value. The output analog voltage of DAC is firstly set with MSB 1 and the corresponding analog value is compared with the input. Consequently the output of comparator is set as 1 or 0. Based upon the output of comparator, SAR logic decides DAC output. Binary search algorithm is used by SAR ADC to perform the conversion operation [21]. Timing is one of the most important factor for accurate functioning of ADC. In SAR ADC, two clocks are used to carry the process of conversion which are generally termed as,

- Global clock
- Bit cycling clock

The global clock has two phases:

- Sample Phase: The period where clock is high is known as the sample phase. Input signal is sampled during this phase.
- Hold phase: The period where clock is low is known as the hold phase. After sampling, the sampled value is held and conversion of the sampled value is performed in this phase.

The conversion operation during the hold phase of global clock is processed out by another clock known as the bit cycling clock. Bit resolution of SAR ADC will decide the number of cycles for the bit cycling clock within the hold period. The bit cycling clock requires N cycles for an N bit SAR ADC. The SAR logic algorithm works on depending upon the output from the comparator.

3.1 SAR Algorithm

Binary search algorithm is implemented in the analog to digital converters based on successive approximations to obtain the precise digital value to the corresponding analog signal which has been sampled.

Bit 1 is determined in first period as MSB (Most Significant Bit). Bit 2 is determined as next most significant bit in next period. Similarly one bit after another is determined until all N bits are decided. Consequently, for N-bit conversion, N cycles are required. Also, a high frequency clock is required to complete the conversion in one conversion cycle.

Procedure for the successive approximation algorithm is as following. Let's consider a random number from 1 to 64. To find that number, the first question that arises is whether this number is greater or smaller than its half scale which is 32. If the number is smaller, then the following thing we have to keep in mind is whether the number is greater or smaller than 16 (middle value of 0 and 32). However, if the number is greater, the next question is whether the number is greater or smaller than 48 (the middle value of 32 and 64). Accordingly, further steps comprise of successively dividing the scales by two till the random number is determined. Figure 12 demonstrates the algorithm.

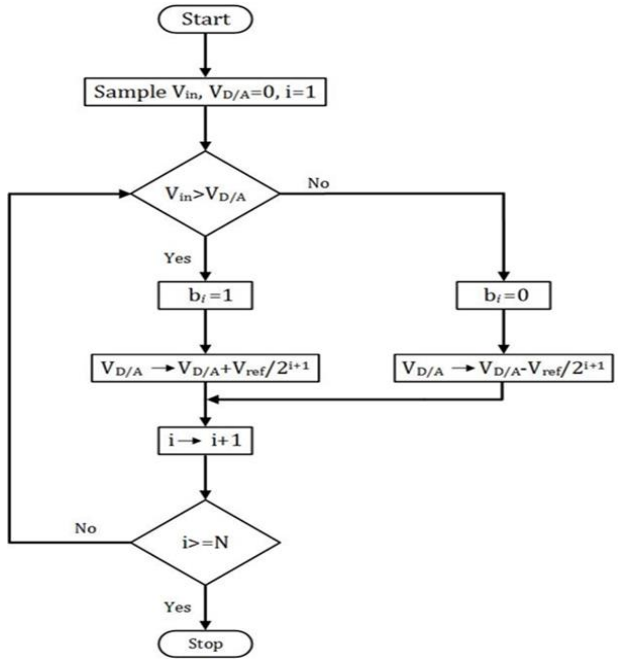


Figure 12. Flowchart of SAR Algorithm

Let's consider a 4 bit SAR ADC operation. As shown in Figure 13, which depicts the successive approximation process of the voltage at the output of the ADC DAC. By setting code to 1000, DAC voltage is set to half of V_{ref} during first clock cycle. After this V_{in} is compared to half of V_{ref} i.e. $V_{ref}/2$ and depending upon the result comparison, MSB is determined. If $V_{in}<V_{ref}/2$, MSB is reset to 0, otherwise it will remain at 1. In this case it will remain at 1. In the next cycle, DAC input is set to 1100 and input voltage is compared to $3V_{ref}/4$. As $V_{in}>3V_{ref}/4$, second most significant bit retains its value. Accordingly, for the next bit DAC input is set to 1110 and upon comparison third bit is reset to 0 as $V_{in}<7V_{ref}/8$. Lastly for determining Least Significant Bit (LSB), DAC input is set to 1101 and as $V_{in}>13V_{ref}/16$, LSB is 1. So final digital code appears to be 1101 in four clock cycles.

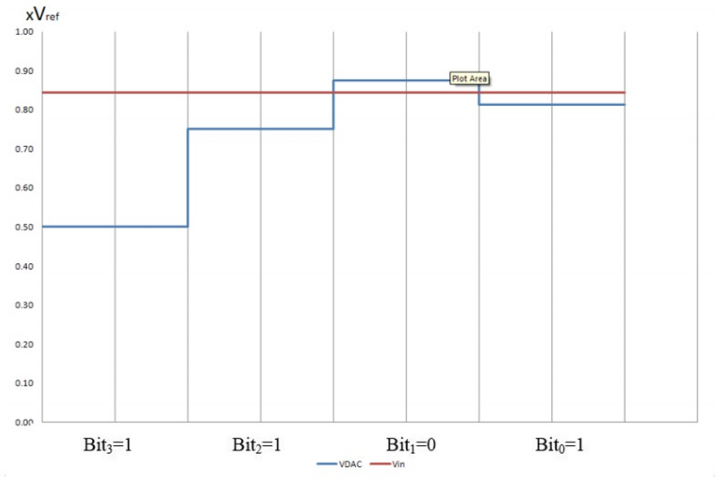


Figure 13. 4-bit SAR ADC Operation

3.2 Different Architectures of SAR ADC

With the advancements in technology, different schemes have been proposed for SAR ADC [22]. Two commonly used architectures of SAR ADC are:

- SAR ADC with separate S/H (Sample and Hold) circuit.
- SAR ADC with capacitive DAC encompassing S/H circuit.

3.2.1 SAR ADC with separate S/H (Sample and Hold) circuit

Figure 14 shows the block diagram of a SAR ADC which includes a sample and hold circuit. In this architecture, comparator's offset does not affect the linearity of the analog to digital converter as it can be modeled as a voltage source in series arrangement with the output of the S/H circuit. It infers adding of the offset to the analog input. Consequently, an offset is present in the overall characteristic. As sample and hold circuit itself is a separate block so it consumes high power which is not preferable for biomedical devices.

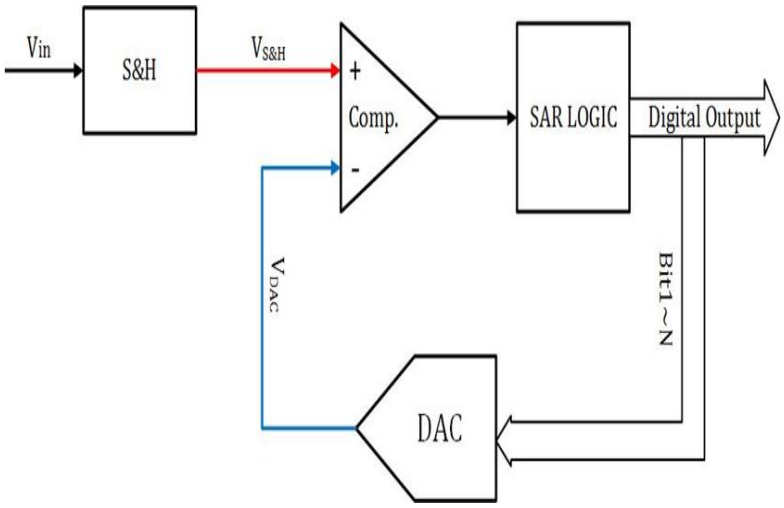


Figure 14. Block diagram of SAR ADC with separate S/H (Sample and Hold) circuit.

3.2.2 SAR ADC with capacitive DAC encompassing S/H circuit

This architecture includes a capacitive DAC which also functions as a sample and hold. The block diagram of the SAR ADC with capacitive DAC encompassing S/H circuit is illustrated in Figure 15. In this architecture, the DAC generally comprises a binary weighted capacitor array. Firstly, analog input is sampled and stored in capacitor array of DAC and its output is compared to common-mode voltage in every conversion. At the comparator's input, common-mode voltage is successively followed by DAC output until it reached to common-mode voltage at the end of every conversion. Due to built-in sample and hold circuit, this architecture consumes less power which makes it a preferable choice.

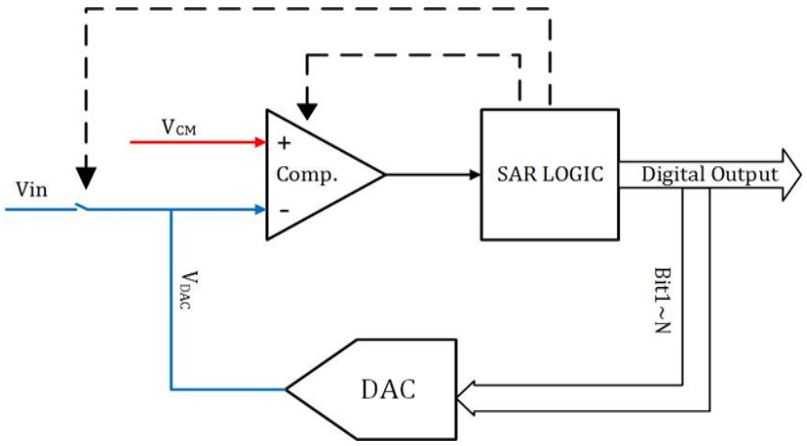


Figure 15. Block diagram of SAR ADC without separate S/H (Sample and Hold) circuit.

3.3 Sample and Hold Block

Sample and hold circuit consists of a switch and a capacitor. This block has two modes, tracking/sampling mode and hold mode. When switch is connected while sampling signal is high, this circuit is in tracking/hold mode and tracks the analog input signal. When switch is disconnected, it is in hold mode. During this mode, this circuit provides a constant voltage at the input of ADC. This block has a great impact on dynamic performance of the ADC.

3.4 Digital to Analog Converter

Digital to analog converter takes input from the output of SAR logic and convert it from digital to analog value. This analog value is than compared with the input value in the comparator. In capacitive DAC encompassing sample and hold circuit, the sampling operation is also performed by DAC. Four main types of digital to analog converter are thermometer code, binary weighted, hybrid, and last but not least is based on a decoder. One of common

types based on switching scheme of DAC is charge redistribution DAC. As compared to resistor based DAC, these DACs induce less mismatch errors and consume less power. Also these DACs are fast in conversion. DACs also consist of many architectures.

Three commonly used architectures are:

- Binary-weighted Capacitor Array
- Two-Stage Weighted Capacitor Array
- C-2C Capacitor Array

3.4.1 Binary-weighted Capacitor Array

This architecture consists of scaled binary capacitors as its name depicts i.e. $2^{N-1}C$, $2^{N-2}C$…4C, 2C, C, C. Figure 16 shows architecture of binary weighted capacitor array. One capacitor is used as a dummy capacitor which makes total value of capacitors $2^{N}C$. Dummy capacitor value is equal to the LSB capacitor. Bottom plates of all capacitors are connected to V_{SS} during reset phase. Depending on provided digital code, switches are either connected to Vref or Ground. This phase is known as redistribution phase. As the resolution of ADC increases, area and power consumption of binary-weighted capacitor array also increases [23].

3.4.2 Two-Stage Weighted Capacitor Array

To lessen the large capacitance size of binary-weighted capacitor array architecture, two-stage weighted capacitor array was proposed. In this method, two smaller binary weighted capacitor are combined through a coupling capacitor whose value is given in (6). Therefore, this methodology occupies

less area, hence consuming less power [24]. Figure 17 illustrates architecture of two-stage weighted capacitor array.

$$\text{Csplit} = \frac{2^{\frac{N}{2}}}{2^{\frac{N}{2}-1}} \qquad (6)$$

3.4.3 C-2C Capacitor Array

This architecture is an elongation of two-stage binary weighted capacitor array. In this approach, the values of the capacitors are radically reduced. So this configuration consumes far less power than other approaches but due to parasitic capacitances, a performance degradation in linearity is observed [25]. Figure 18 shows architecture of C-2C capacitor array.

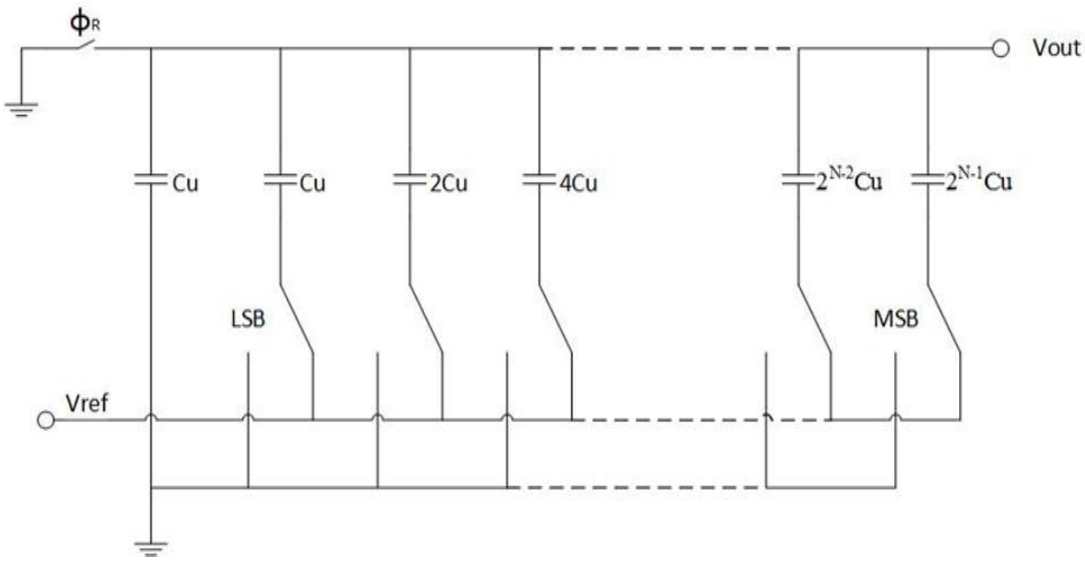


Figure 16. Architecture of Binary Weighted Capacitor Array.

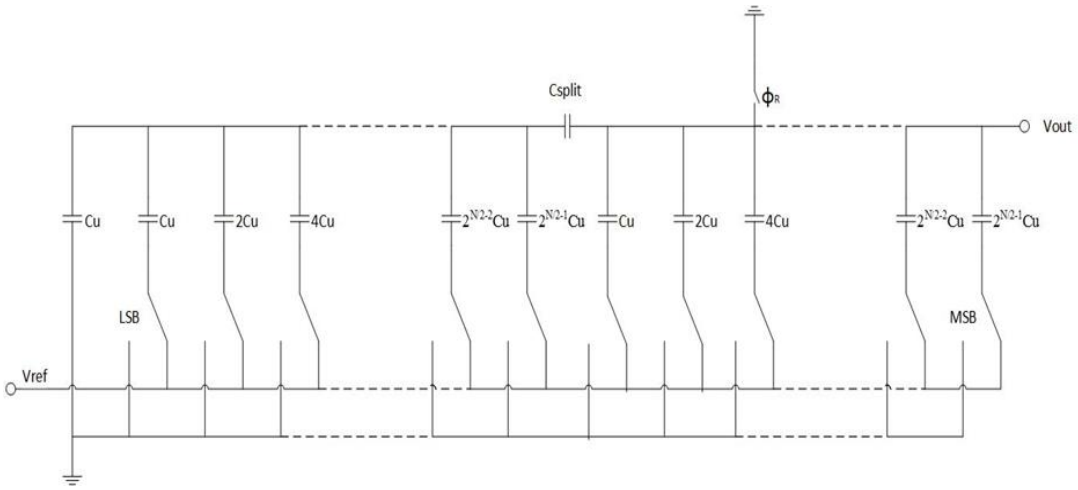


Figure 17. Architecture of Two-Stage Weighted Capacitor Array

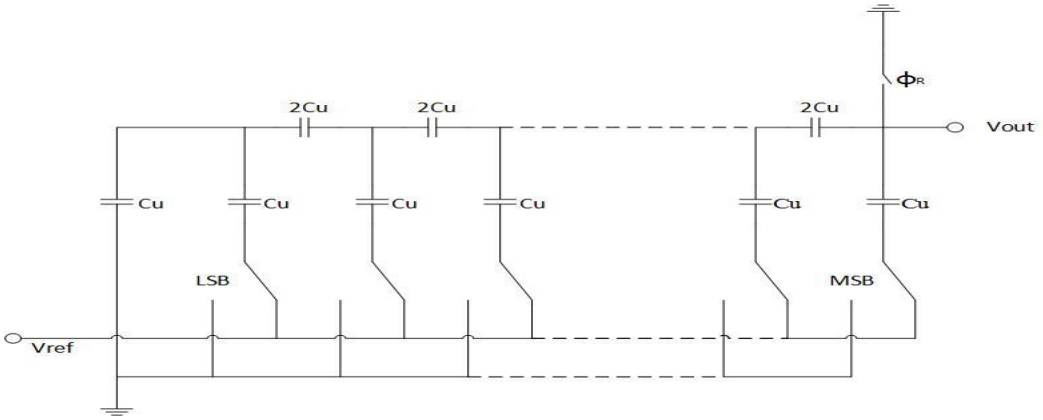


Figure 18. Architecture of C-2C Capacitor Array

Considering power constraints of biomedical devices, binary weighted DAC is the most appropriate choice for low power consumption. Further, binary weighted DAC can be categorized into current signal's binary array or charges' binary array. Former array makes use of voltage driven R-2R techniques which entails vigilant control of the on-resistance proportions in the MOS switches over a vast range of values and can be subjected to complications

during fabrication process. On the contrary, binary weighted array of charges has a comparative advantage over former one as capacitors are easily fabricated in metal gate technology. Also, when a MOS device is implemented as a charge switch, the value of offset voltage is characteristically zero and when it is employed as an amplifier, its input resistance is very high. This feature as well provides an edge to binary weighted array of charges, making capacitors and charges more suitable as the precision component and medium of work respectively.

Power efficiency of SAR ADC is highly reliant on switching scheme of capacitive DAC array. Numerous works have taken this factor into account and have achieved a good reduction of energy through a variety of design approaches [26]-[29]. Switching scheme implemented in this work has been derived from monotonic switching scheme [27]. For an n-bit conventional SAR ADC, the average switching energy is

$$E_{avg,conventional} = \sum_{i=1}^{n} 2^{n+1-2i} (2^i - 1) CV_{ref}^2 \qquad (7)$$

The average switching energy for n-bit SAR ADC using monotonic switching scheme can be expressed as

$$E_{avg,monotonic} = \sum_{i=1}^{n-1} \left(2^{n-2-i}\right) CV_{ref}^2 \qquad (8)$$

The difference between conventional and monotonic switching procedure is depicted in Figure 19 and 20, where in former switching scheme common mode voltage of the reference DAC does not drop from half of reference value to ground while in latter scheme it does. In this work, half scaled reference based monotonic switching scheme has been implemented.

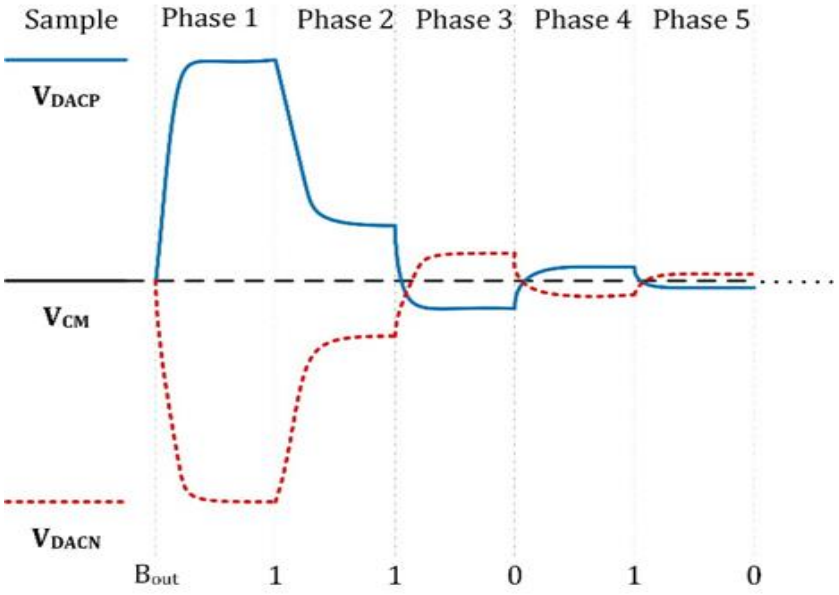


Figure 19. Waveform of conventional switching scheme.

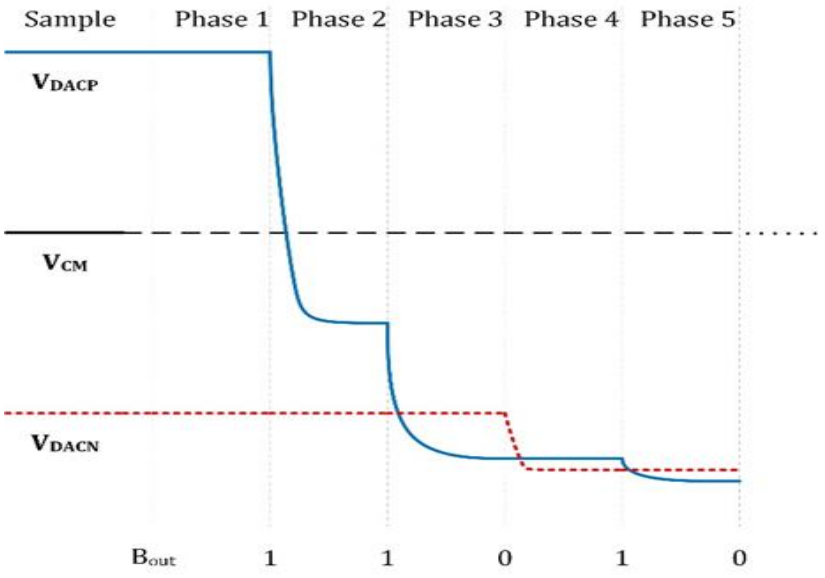


Figure 20. Waveform of monotonic switching scheme.

3.5 Comparator

Comparator compares two voltages analog values. In case of SAR ADC, it compares the sampled analog input to the output of DAC and generates digital output either 0 or 1 which is used by SAR logic.

Comparators can be classified into two categories namely static comparators and dynamic comparators. In the former type, every gate's output is either connected to supply voltage or ground through a less resistive path at every point in time excluding the time of switching transients. This type of comparator is used in moderate speed applications and is less prone to noise but it has static power dissipation which occurs due to short circuit power dissipation. Contrarily, the latter type is reliant on short term storage of signals on the capacitance of circuit nodes having high impedance. Though this type is more sensitive to noise but it is useful for medium to high speed applications. Moreover this type does not consume static current by using a clock input which does not allow the flow of current between supply voltage and ground, eventually making it more power efficient.

A simplified dynamic comparator consisting of two operational phases of reset and latch, consumes energy as described in (9) as a function of signal to noise ratio (SNR) from comparator and ADC resolution n.

$$\Delta E_{COMP} \cong \frac{2kT}{3} \cdot SNR_{COMP} \cdot [n^2 + 12n + 2] \qquad (9)$$

Dynamic offset, delay, input inferred noise and large power consumption are the parameters of the comparator which can degrade the performance of the ADC particularly when designing an ADC for biomedical implant devices. Specific design considerations can improve the overall performance. Possible

solutions for improving the dynamic offset includes reduction of voltage of the input pair or increasing the size of comparator. However these techniques will lead to slow comparison speed and enormous power consumption respectively, substantiating the fact that associated design tradeoffs and constraints are highly related to the realm of ultra-low power circuits [30]. Therefore a comparator topology that has a potential of reducing kickback noise, working at low supply voltages with low power consumption and optimizing a balance between power and common mode voltage and speed and offset is a preferable consideration for biomedical implant devices applications, is implemented in this ADC design.

3.6 SAR Logic

SAR ADC is based on a binary search algorithm. The binary search algorithm technique is accomplished by a digital controller circuit which is successive approximation register (SAR). Two primary designs followed for designing SAR logic circuit were proposed in [31] and [32]. Former design makes use of a ring counter and a shift register and for an n-bit ADC, at least 2n flip-flops are employed. While the latter design uses some combinational logic and comprises of n flip-flops, half of former technique. Depending upon output of comparator. SAR control logic determines bits sequentially. Figures 21 and 22 show the architecture of SAR logic block for aforementioned designs.

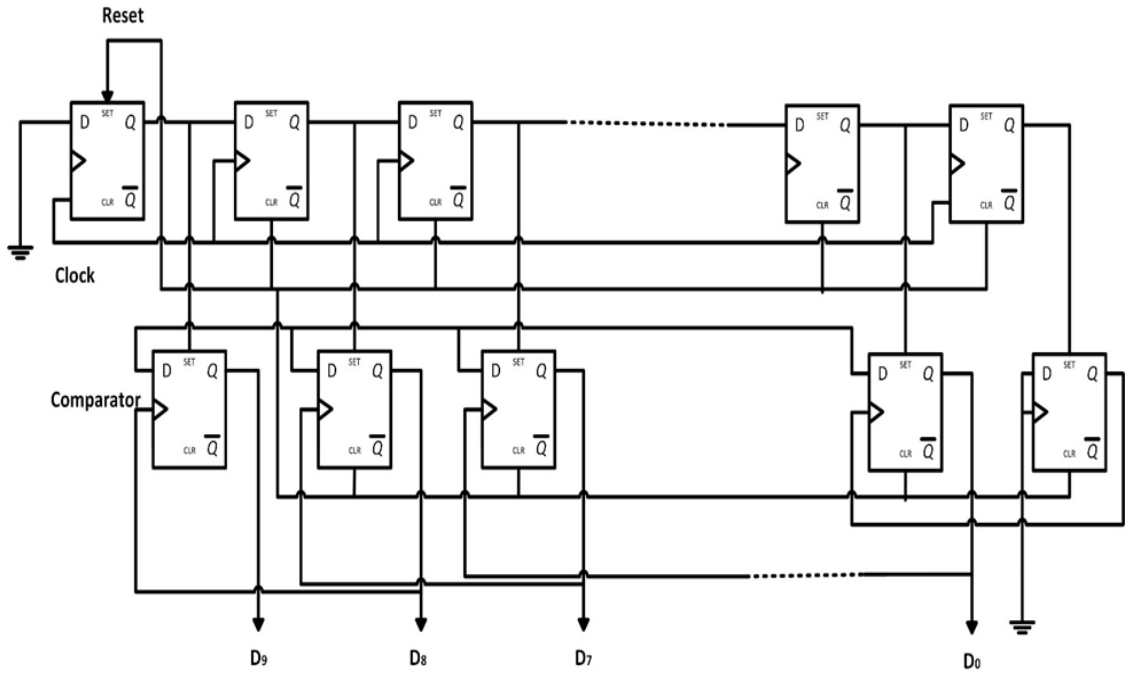


Figure 21. SAR logic block architecture proposed by Anderson.

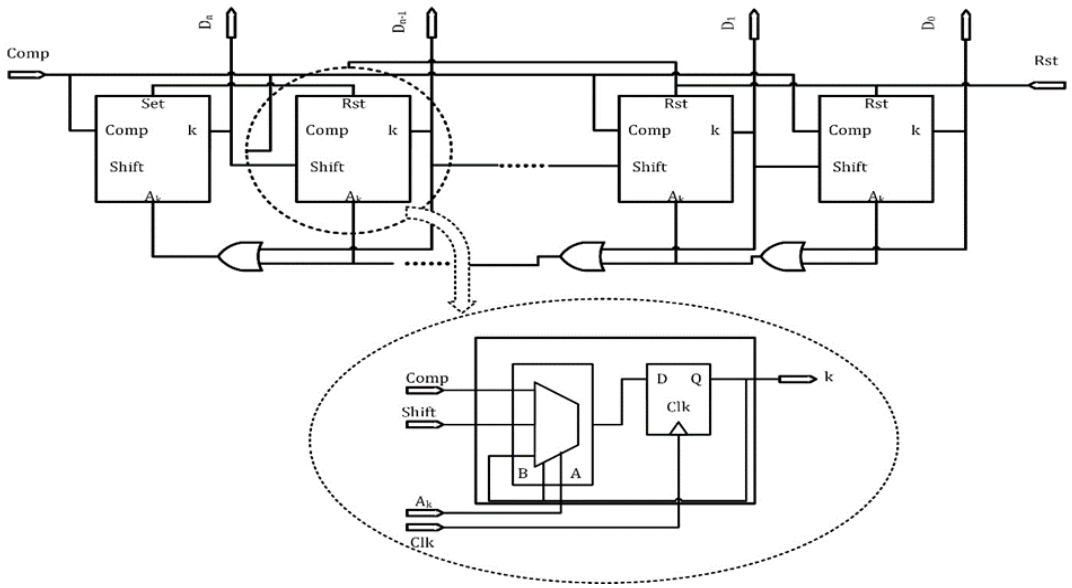


Figure 22. SAR logic block architecture proposed by Rossi.

Chapter 4: Proposed System

Uncomplicated structure, minimum analog circuitry and low power consumption characteristics have brought SAR ADCs into limelight once again over past years for employing in biomedical implant devices. Charging and discharging of capacitive DAC network, SAR control logic and comparator are the primary power consumption sources in a SAR ADC. Various low power SAR ADC designs have been proposed but still there are many challenges for ultra-low power operation due to downscaling of CMOS technologies. Since biomedical signals usually range from few Hz to several kHz, nonlinearity can occur with the increase in resolution of SAR ADC. In the course of long conversion process, sampled voltage is discharged via sampling switch's leakage current. Therefore, in applications involving low sampling rate, maintenance of a sampled voltage is one of the significant design concerns for ADCs. Besides, area of a binary weighted digital to analog converter (DAC) expands exponentially with increase in resolution. Linearity and power consumption performance of a SAR ADC is reliant predominantly on capacitive DAC. In terms of leakage current, design with enhanced control voltages has been implemented to reduce the leakage current. Also area of binary weighted capacitive array is reduced by splitting the capacitor array.

4.1 Capacitive DAC Array Switching Scheme

The implemented switching scheme is performed in two phases. In the first phase, most significant bit (MSB) is determined by using shifting level technique. In the second phase, half scaled reference based monotonic switching is used for least significant bits (LSBs). By using this scheme,

number of capacitors and switching energy is reduced considerably. Figure 23 shows a 3-bit differential SAR ADC implementing this switching scheme. Firstly, differential input signal is sampled using sampling switches on the top plates of differential capacitor arrays. In the meantime, bottom plates of capacitors are connected to half scaled reference voltage (V_{REF}). In the next phase, comparator makes the first comparison while sampling switches are turned off without consuming any switching energy. Negative input voltage which is sampled at the bottom plates of capacitor array are connected to reference voltage and rest of capacitor array remains same after the MSB has been acquired. Consequently, level of voltage of capacitors on negative voltage side is shifted by half of reference voltage. No switching energy is consumed during this process. Different reference voltages for capacitor arrays are chosen according to Table 1 once the MSB comparison is completed. When MSB=0, positive capacitor array will have $V_{REFP}= V_{REF}$ and $V_{REFN}=\frac{V_{REF}}{2}$. On the complementary side, capacitor array will have $V_{REFP}= \frac{V_{REF}}{2}$ and $V_{REFN}= V_{GND.}$ Moreover, when MSB=1, positive capacitor array will have $V_{REFP}= \frac{V_{REF}}{2}$ and $V_{REFN}= V_{GND}$ and negative capacitor array will have $V_{REFP}= V_{REF}$ and $V_{REFN}=\frac{V_{REF}}{2}$.

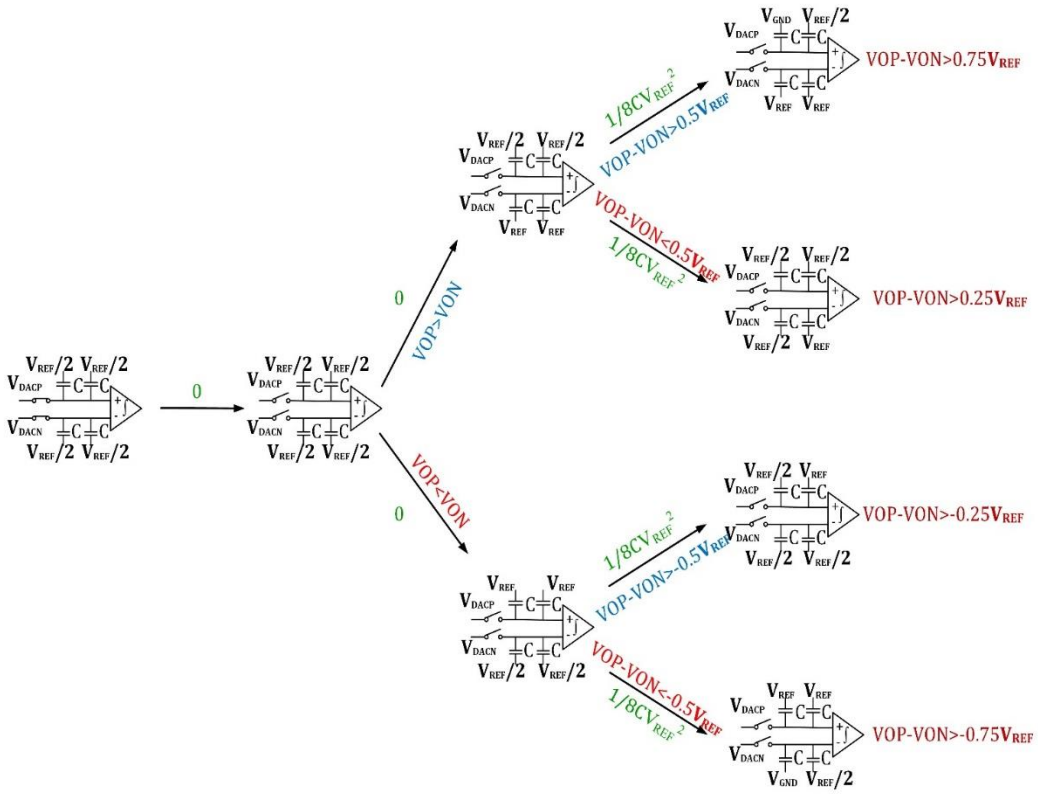


Figure 23. Half scaled reference voltage based monotonic switching scheme of 3-bit ADC.

Depending upon the output of comparator, the corresponding capacitor on positive voltage side switches from $\frac{V_{REF}}{2}$ to ground or from V_{REF} to $\frac{V_{REF}}{2}$ and other one remains the same. Till the LSB is determined, this process is repeated. Less energy is consumed when monotonic switching is performed as for each bit cycle there is only one capacitor switch. Figure 24 shows the variation of reference voltage levels in the implemented switching scheme. For an *n*-bit ADC, the average switching energy for the implemented scheme can be expressed as

$$E_{avg} = \sum_{i=1}^{n-2}\left(2^{n-i-5}\right) CV_{ref}^2 \qquad (10)$$

In comparison to conventional and monotonic switching scheme, the implemented switching procedure consumes very less power.

Table 1 Different reference voltages decision for differential capacitor array reliant on MSB value

	MSB=0		**MSB=1**	
Differential Input	V_{DACP}	V_{DACN}	V_{DACP}	V_{DACN}
V_{REFP}	V_{REF}	$\frac{V_{REF}}{2}$	$\frac{V_{REF}}{2}$	V_{REF}
V_{REFN}	$\frac{V_{REF}}{2}$	V_{GND}	V_{GND}	$\frac{V_{REF}}{2}$

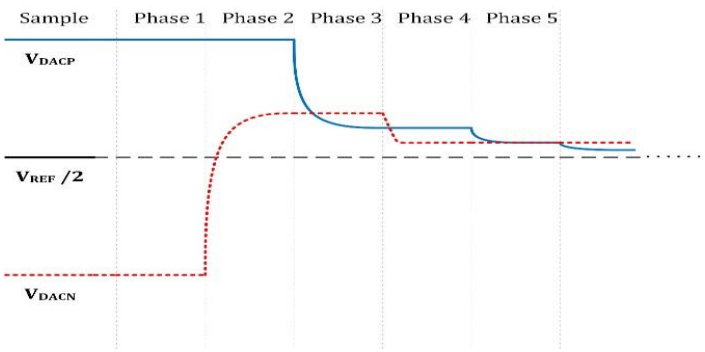


Figure 24. Waveform of half scaled reference voltage based monotonic switching scheme.

4.1.1 Capacitor Array

A binary weighted capacitor array offering more linearity has been implemented. The power consumption of capacitive DAC array is directly proportional to the size of unit capacitor C_u. In order to determine the smallest value of C_u, matching accuracy of required capacitor, thermal noise power *(kT/C)* and technology design rules and parasitic capacitance are taken into consideration. In this design a unit capacitor of 20fF is chosen. Metal-insulator-metal (MIM) capacitors have been implemented as they have small parasitic capacitance.

.2 Comparator Design

In this work, four different architectures are proposed for comparator design. Since, prime focus for this research is low power consumption, the comparator with least power consumption is chosen for SAR ADC.

4.2.1 Dynamic Latched Comparator

Figure 25 depicts a dynamic latch comparator. When the clock signal is low, reset transistors are turned on and output nodes along with drain nodes of input transistors are charged to supply voltage. At this phase, M_{11} is off, so no current flows through the circuit. During high clock signal, reset transistors ae turned off and M_{11} is turned on. Depending upon V_{in}, inverters of cross coupled circuitry inside the latch receive different quantity of current and start to regenerate the output of comparator. In other words, drain voltages of transistor M_9 and M_{10} start to release from V_{DD} to V_{SS} with altered rates based upon V_{in}. When drain voltage of any of these transistors is below supply voltage subtracting threshold voltage, inverter's NMOS transistor is switched

on and discharge starts from the output node and positive feedback is triggered. When the output node equals to V_{DD}- V_{th}, inverter's PMOS transistor is switched on. Subsequently, the output voltage is redeveloped and after regeneration stage one of the outputs is 0 while the other is 1. In this configuration, the PMOS switch transistors (M_2, M_3, M_5, and M_6) which charge input transistors' drain node to V_{DD} in the course of the reset stage, enhance the time period that input transistors are in saturation region in the course of regeneration stage. As a consequence, higher gain is achieved. Large kickback noise occurs at drain nodes of input transistors due to voltage variations. Moreover, it is also produced with the variation of the operation region of input transistors. In the reset phase, differential input pair transistors are not on. When the comparator moves in the assessment phase, V_{DS} is high and transistors are in saturation region, then these nodes make the transistors to go in triode region as they are discharged to zero in the regeneration stage. So as to hold the output of the comparator during the reset stage, a NOR type Set-Reset Latch is used as shown in Figure 26. In this design there is a tradeoff between speed and power consumption [33].

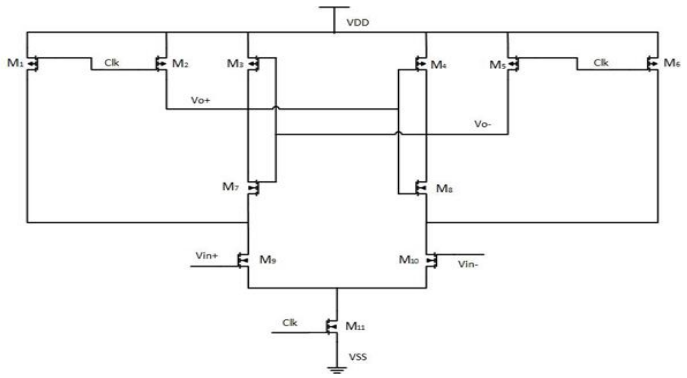


Figure 25. N-type latched comparator circuit.

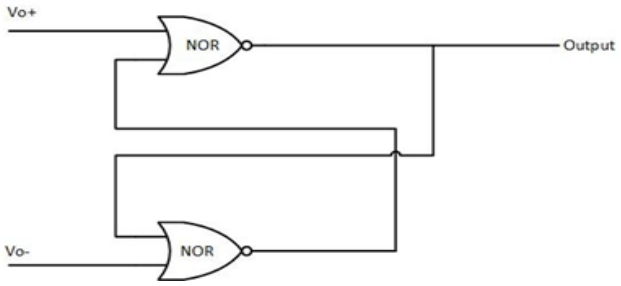


Figure 26. NOR type SR Latch circuit.

4.2.2 Double Tail Dynamic Latched Comparator

A double tail dynamic latched comparator is introduced in order to overcome the dynamic and the modified dynamic latched comparator problems [34]. As the name suggests, the structure consists of two tails, one at input-stage, while the other in latching stage (see Figure 27). Due to the lower stacking of this structure, the circuit is capable of working at lower supply voltages. Due to the presence of two tails, large current flows through the circuit that results in fast latching in latching stage which is independent of the common mode voltage of the circuit also it provides a smaller current at the input stage that provides lower offset and noise. During the reset phase *(Ø = 0)*, driver transistors M_9 and M_{10} charges M_{11} and M_{12} to (V_{DD}). In accordance to that, V_{out+} and V_{out-} will be high. As the reset phase ends, the tail transistors M_3 and M_{13} changes to *ON* state. At the drains, the CM voltage drops at a rate defined by (I_{M3}/ $C_{differential\ pair\ drains}$) and above this, an input dependent differential voltage (ΔV_{Di}) will be created. The additional stage created by M_{11} and M_{12} goes (ΔV_{Di}) to the cross coupled inverters providing shelding effect between the input and output, due to which kickback noise is reduced. When the CM Voltage at the differential pair nodes is not sufficient for M_{11} and M_{12} to switch

its drain to ground, the inverters start reproducing the voltage difference. The ideal operating point and various phases can be calibrated by modifying the transistor W/L ratio. The double tail topology provides better tradeoff between speed and offset, irrespective of power and common mode voltage. Moreover it is well suited for low-voltages low-power operation. Thus, this comparator design is well suited for low-power, medium-speed and average dynamic range applications, in comparison to the other mentioned comparator circuits. This is achieved due to the double tail and less stacking structure.

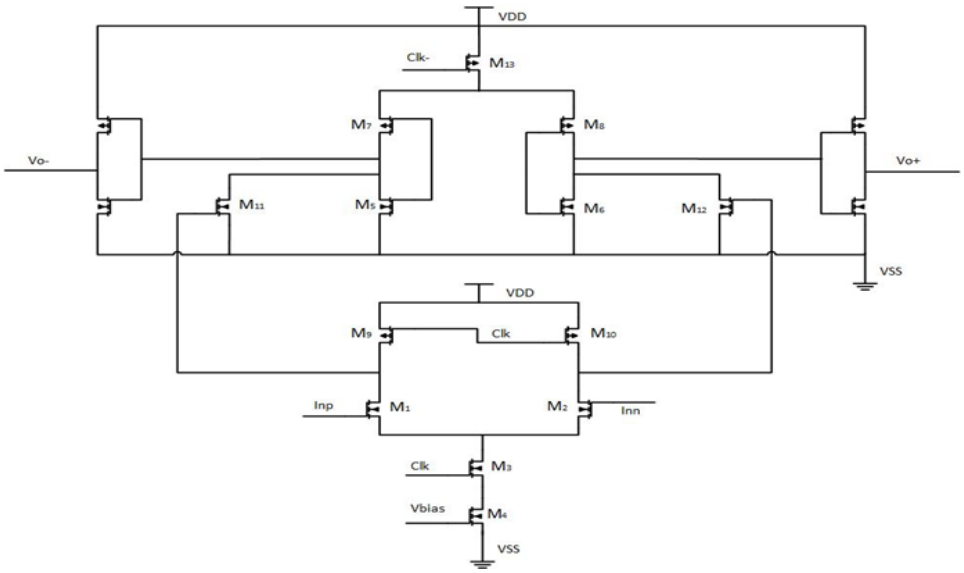


Figure 27. Double Tail Dynamic Latched Comparator.

4.2.3 Regenerative Latch Comparator

The architecture of this comparator contains a regenerative latch followed by an SR latch and inverters. The regenerative latch operates on a clock and performs the actual comparison [35]. The comparator architecture selected is

shown in Figure 28. In this architecture, as the clock goes low, $M_{10,11}$ goes on which charges the output node capacitance. Meanwhile, M_5 is switched off and so does the path between the input transistors. As the clock goes high M_1 and M_2 transistors are switched on providing a path towards ground. As soon as M_5 goes on, sources of the input transistors are connected to the ground. Due to which, whenever there is a input signal at the gates of the input transistors, it causes the output capacitances to discharge at different rates. The flow of current in the circuit relies on the voltage applied to it, such that, when V_{inP} is larger V_{outN} falls rapidly, until it goes below $V_{DD} - |V_{ThersholdP}|$ which M_9 to produce a logic "1" at V_{outP} and a "0" at V_{outN}.

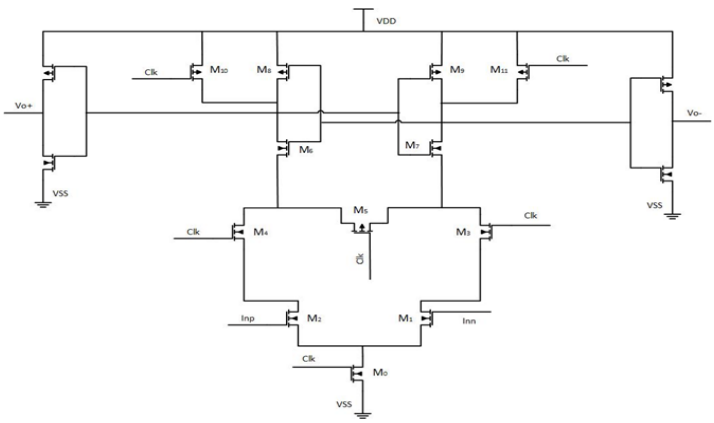


Figure 28. Regenerative Latch Comparator.

4.2.4 Comparator with Biasing Topology

The schematic of two-stage dynamic comparator employed in this ADC is depicted in Figure 29. It consists of a preamplifier and a latch stage. First stage amplifies the input signal and blocks the kickback noise. Though output of the preamplifier stage results in a larger output signal as compared to the input

signal but is inadequate to operate the digital circuitry. Second stage is required to amplify the signal to logic. To undergo an ultra-low voltage operation along with improving dynamic offset, a reliable method is to insert a biased CMOS along with the body biasing topology. The operation of comparator fully exploits two modes of clock. When the clock signal ($\emptyset$) is high, nodes X_p and X_n are pre-charged to ground (V_{SS}). On the other hand, Y_p, Y_n, Out_p and Out_n are pre-charged to supply voltage (V_{DD}). Conversely, when the clock is low, first stage of the comparator amplifies the difference of X_p and X_n proportionate to V_{inp} and V_{inn} and common mode voltage of X_p and X_n nodes escalates. When the transistors of latch stage (M_{11} and M_{12}) are switched on, the regeneration of cross coupled inverter initiates to figure out the values of V_{outp} and V_{outn}. The preamplifier stage takes full leverage of the transistor M_1 which is a source for biased current in contemplation of reducing dynamic offset. Body biasing technique has been applied in both preamplifier and latch phase. PMOS transistors of former phase (M_3 and M_4) and NMOS transistors of latter phase (M_{11} and M_{12}) are biased with ground and supply voltage respectively. The charging delay that occurs prior to initiation of regeneration of cross coupled inverter can be reduced by applying body biasing to input transistors with low threshold voltages in both stages of the comparator. In addition to that, the transistors of cross coupled inverter are also body biased during second stage of the comparator in pursuance of minimizing the delay caused by regeneration. In this comparator, considering threshold voltage as a function with increased tail current of latch stage, input transistors with body biasing of both stages can reduce charging delay for X_p and X_n nodes linearly and charging delay for Out_p and Out_n nodes exponentially.

Moreover, considering threshold voltage as a function with increased tail current of latch stage along with effective trans-conductance of NMOS load transistors, body biasing of cross coupled inverter can reduce charging delay for Out_p and Out_n nodes linearly and regeneration delay exponentially. Tail current in subthreshold region is given by

$$I_{tail} = \mu C_{ox} \frac{W}{L} (n-1) V^2{}_T e^{\left(\frac{V_{gs}-V_{th}}{nV_T}\right)} \left(1 - e^{\left(\frac{-V_{ds}}{V_T}\right)}\right) \qquad (11)$$

Where n is the slope factor of threshold and V_T is the thermal voltage. This comparator topology offers fast and low power operation.

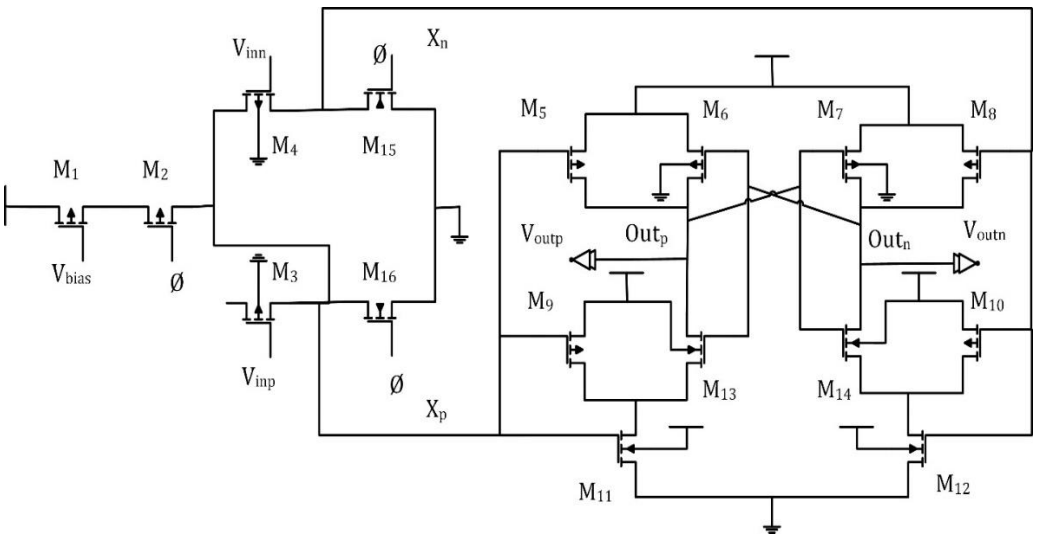


Figure 29. Two stage ultra-low power dynamic comparator with body biasing technique.

4.3 SAR Logic Design

Digital control circuitry comprises of successive approximation registers (shift register and latches), control logics and a clock generator. As sampling rate is

low, therefore instead of using dynamic logic, static one is used to avoid charge leakage. A latch has less transistor count so it is a preferable choice for reducing power consumption. The control logics control the switches of capacitive DAC array and are composed of simple logic gates. Figure 30 depicts the block diagram of successive approximation register which is composed of D-Flip-flops. The schematic of D-Flip-flop and latch is shown in Figure 31 and 32 respectively.

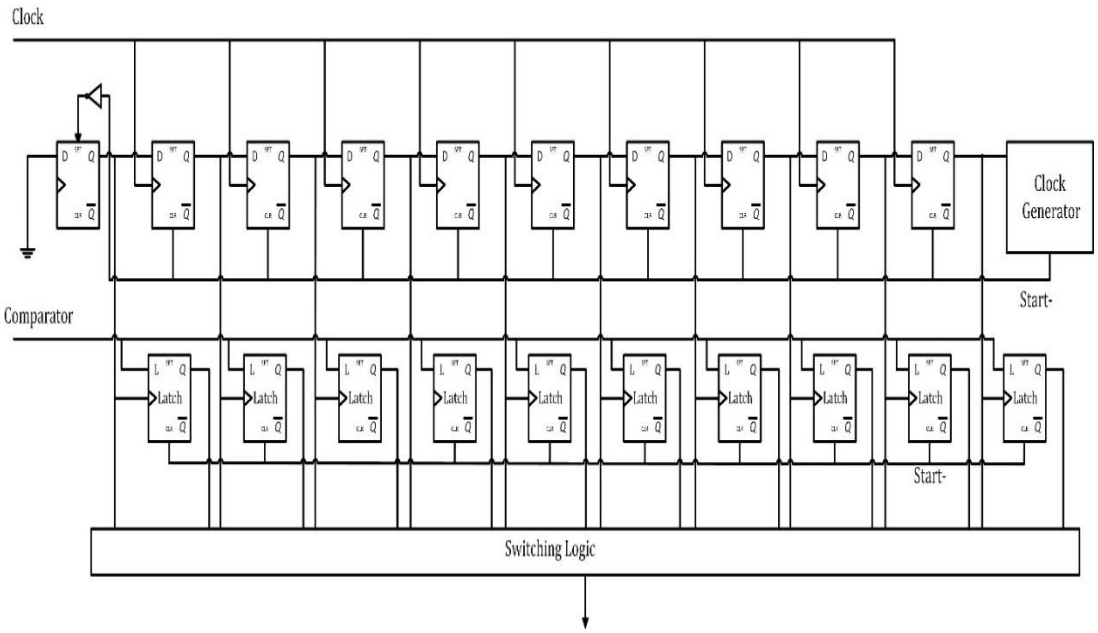


Figure 30. SAR digital logic.

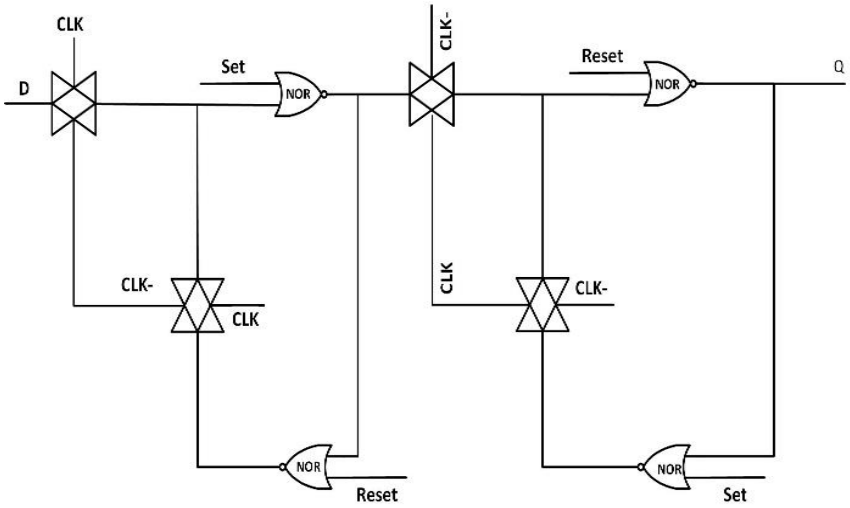


Figure 31. Schematic of D-Flip-flop circuit.

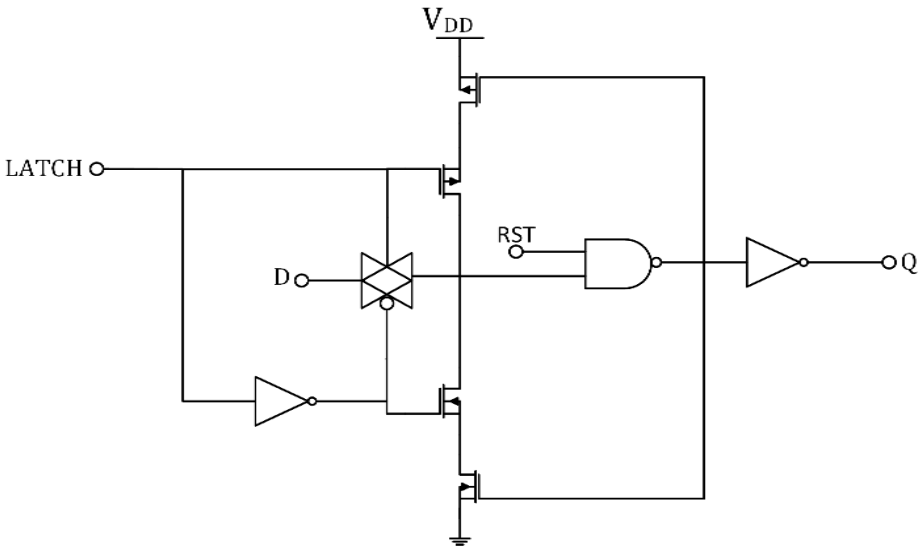


Figure 32. Schematic of Latch circuit.

Chapter 5: Results and Discussion

The SAR ADC has been verified at a transistor level simulation, using a 180-nm technology mode. Simulated at a frequency of 500 kS/s, the 10-bit SAR ADC specifically designed for biomedical devices aims for ultra-low power consumption. A test bench was set up for measuring results of the SAR ADC. The typical supply voltage is 1.8 V according to 180-nm CMOS technology. The input analog signal has a range from 0 to the reference voltage. The measured differential non-linearity (DNL) and integral non-linearity of the implemented ADC are depicted in Figure 33 and 34. Figure 35 shows the measured FFT spectrum at an input frequency close to 237 kHz at a supply voltage of 1.8V and 500 kS/s sampling rate. The measured SNDR and SFDR are 55.8 dB and 63.4 dB respectively. The resultant ENOB is 8.57 bits. Measurements by decreasing the input frequency are also taken into consideration and an increase in the measured values of SNDR and SFDR are observed. Moreover, if sampling rate is increased, performance degradation is observed.

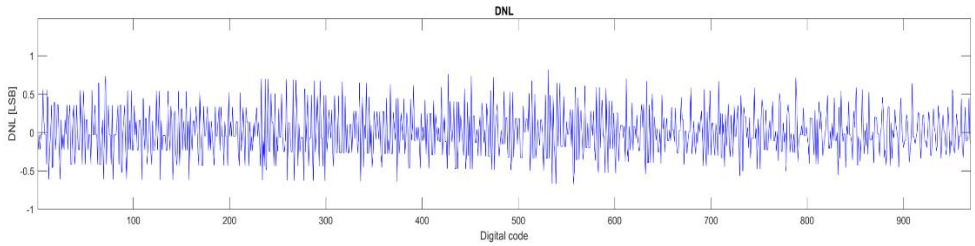


Figure 33. Measured DNL

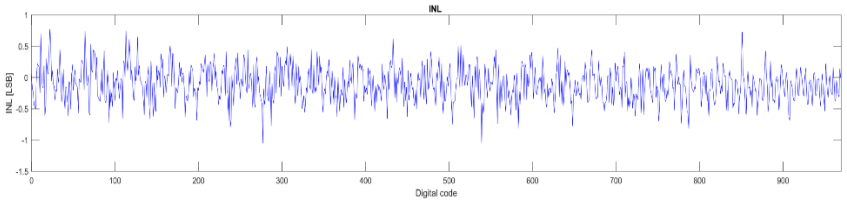


Figure 34. Measured INL

Three main factors contribute to power consumption: dynamic power consumption, direct path consumption, and leakage power consumption. The power consumption of direct path consumption and leakage power consumption is low. Hence, the major factor affecting power consumption is dynamic power consumption. Dynamic power is affected largely by supply voltage; therefore, measurements by decreasing the supply voltage can also be taken into consideration. The total power consumed by the designed SAR ADC for 500 kS/s is approximately equal to 3.6 μW.

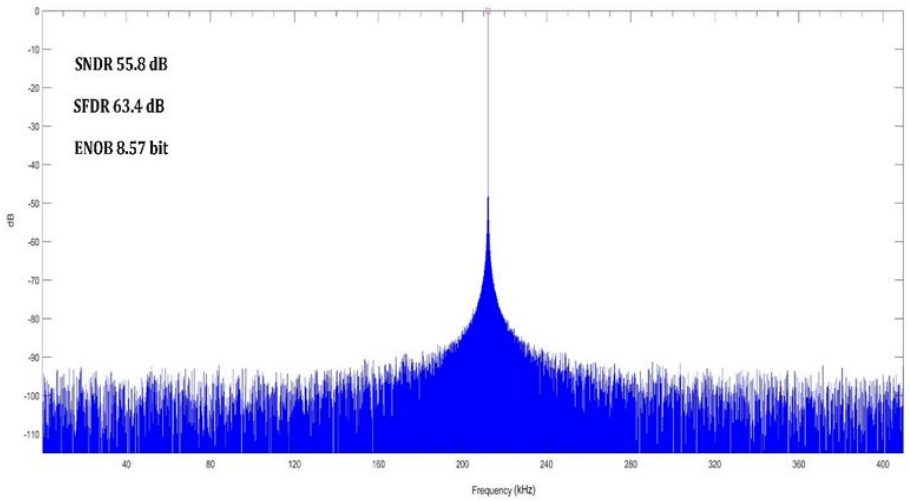


Figure 35. Measured FFT spectrum at 237 kHz input frequency.

Table 2 summarizes the comparison of proposed SAR ADC with other works with almost similar speed and resolution.

Table 2 Comparison with other works

Design	[36] ADC for wireless micro sensors applications	[37] Rail to Rail 8-bit SAR ADC	[38] SAR ADC with Splitting Comparator	[39] Low Power SAR ADC	This Work
Technology (nm)	180	180	180	180	180
Resolution (Bits)	12	8	10	8	10
Sampling Rate (kS/s)	100	400	500	500	500
SNDR (dB)	65	47.4	58.4	46.92	55.8
SFDR (dB)	71	58.9	75	62.69	63.4
ENOB	10.55	7.731	9.4	7.5	8.57
Power (µW)	25	6.15	42	7.75	3.6
DNL (LSB)	+0.58/-0.66	+0.26/-0.9	+0.76/-0.8	+0.17/-0.24	+0.5/-0.5
INL (LSB)	+0.68/-0.56	+0.5/-0.53	+0.76/-0.76	+0.31/-0.28	+0.54/-0.6

Figure 36 shows the power breakdown by percentage of key building blocks of SAR ADC implemented in this paper representing the power consumed by each block.

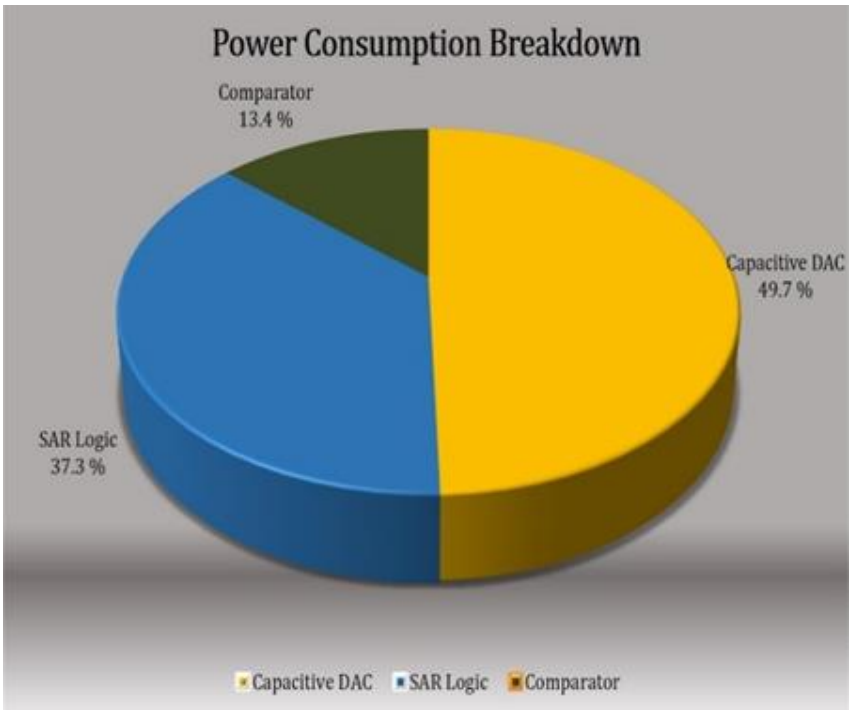


Figure 36. Power consumption breakdown

Chapter 6: Conclusion

In this thesis, a 10-bit 500 kS/s SAR ADC for biomedical implant devices is presented. A binary weighted split capacitor DAC architecture and a half scaled reference voltage based monotonic switching scheme is implemented to reduce total capacitor count, area and power consumption. An ultra-low power consuming dynamic comparator with body biasing technique is employed in contemplation of complying with power limitations of implantable biomedical devices. The implemented switching scheme leads to smaller total capacitance and low switching energy. In addition to that, ultra-low power comparator design is employed. The measurement results show that the ADC achieves an ENOB of 8.57 bit and consumes only 3.6μW at 500 kS/s.

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