August 2019
Master's Degree Thesis

12-bit 3.072GS/s Time-Interleaved Pipelined Analog-to-Digital Converter for Full-Digital Wideband TV Receiver Application

Graduate School of Chosun University
Department of Information and Communication Engineering

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Advisor: Prof. Goang Seog Choi

A thesis submitted in partial fulfillment of the requirements for a master's degree

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Waleed Hussain Siddiqui의
석사학위논문을 인준함

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LIST OF ABBREVIATIONS AND ACRONYMS

ATSC	Advanced Television Systems Committee
ADC	Analog-to-Digital Converter
DOCSIS	Data Over Cable Service Interface Specification
DVB	Digital Video Broadcasting
DFF	D-Type Flip Flop
DLL	Digital Lock Loop
DNL	Differential Non-Linearity
ENOB	Effective Number of Bits
ERBW	Effective Resolution Bandwidth
GBW	Giga-Bandwidth
IGE	Interstage Gain Error
INL	Integral Non-Linearity
MPCG	Multi-Phase Clock Generation
MCLK	Master Clock
MDAC	Multiply Digital-to-Analog Converter
SAR	Successive Approximation Register
SR	Shift Register
SNDR	Signal-to-Noise and Distortion Ratio
SFDR	Spurious-Free Dynamic Range
TG	transmission gate
TI-ADC	Time-Interleaved ADC
TSPC	True Single Pulse Clock
Σ-Δ	Sigma-Delta

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ABSTRACT

12-bit 3.072GS/s Time-Interleaved Pipelined Analog-to-Digital Converterfor Full-Digital Wideband TV Receiver Application

Waleed Hussain Siddiqui
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The performance of a fully digital wideband receiver is highly dependent on the performance of the analogue-to-digital converter (ADC) used. Such applications require ADCs to operate at ultra-high speeds with high accuracy for inputs ranging from 40 MHz to 1 GHz. Conventional solutions either use filters and mixers to extract the frequency of interest, and convert it using a low-speed ADC or use a single ultra-high-speed Flash converter. Both of these solutions consume ultra-high power and require complex circuitry, which expands exponentially with the converter resolution. In this work, a 12-bit 3.072 GS/s time-interleaved pipeline ADC is proposed. In total, 32 pipeline ADCs, each with a sampling rate of 96 MS/s, are interleaved in the time-domain to achieve an overall sampling rate of 3.072 GS/s. In addition to the potential energy-saving capabilities of a Time-interleaving structure, the circuit adopts amplifier-sharing in sample-and-hold circuits, further improving the power efficiency. To account for interleaving mismatches, the circuit uses a pure background calibration technique, maintaining the system linearity and spectral efficiency. The proposed design achieves SNDR of 53.65 dB and SFDR of 69.04 dB, while consuming 820 mW of power at a 1.2-V supply, resulting in a FoM of 0.67 pJ/conv.-step.

한 글 요 약

전-디지털 광대역 TV 수신기 응용을 위한 12비트 3.072GS/s 시간-간격 파이프라인 아날로그-디지털 변환기

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전-디지털 광대역 수신기의 성능은 사용되는 ADC의 성능에 따라 크게 달라집니다. 이러한 응용 프로그램은 ADCs는 높은 정밀도와 함께 입력 40MHz부터 1GHz까지 범위에 걸친 초고 속도에서 작동할 것을 요구합니다.기존 솔루션은 필터와 믹서를 사용하여 관심 빈도를 추출하고, 저속 ADC를 사용하여 변환하거나 단일 초고속 플래시 ADC를 사용합니다.이 두 솔루션은 모두 초고전력을 소비하며, 변환기의 분해능에 따라 기하급수적으로 확장되는 복잡한 회로를 필요로 합니다.이 논문에서는 12비트 3.072 GS/s의 시간-간격 파이프라인 아날로그-디지털 변환기가 제안됩니다.총 32개의 파이프라인 아날로그-디지털 변환기들(각각 96개의 샘플링 속도)가 시간 영역 내에 인터리빙되어 전체 샘플링 속도가 3.072 GS/s입니다. 이 회로는 시간-간격 구조의 잠재적 에너지 절약 기능 외에도 샘플링 및 홀드 회로에서 앰프 공유를 채택하여 전력 효율을 더욱 향상시킵니다.회로에서는 시간-간격 불일치를 해결하기 위해 순수 백그라운드 보정 기법을 사용하여 시스템 선형성과 스펙트럼 효율성을 유지합니다.제안된 설계는 SNDR이 53.65dB이고 SFDR이 69.04dB인 반면, 1.2V 공급 장치에서 820mW의 전력을 소비하여 FoM이 0.67pJ/con-step이 됩니다.

I. INTRODUCTION

A. Motivation

With the rapid advancements in technology, the desirability of digital systems has conceivably boomed, owing to their flexible nature [1]. At present, most communication and control problems are addressed using digital approaches. As with other communication applications, digital circuits have long been used in electronic warfare receiver applications. Such applications require very large, instantaneous bandwidths, and their input spectrum may range from DC to thousands of megahertz to satisfy their operational requirements. Traditional (analogue) wideband receivers used crystal video detectors for converting RF signals into video. However, the use of crystal video detectors sacrifices the carrier frequency and signal phase value [2].

With the advent of high-speed analogue-to-digital converters (ADCs), fully digital wideband receivers have attained significant dominance over traditional receivers. In contrast to analogue wideband receivers, a digital wideband receiver replaces the crystal detector with an ADC, as a result of which all the information remains preserved during the conversion. Moreover, as the output of the ADC is digital, post-conversion processing will take place in the digital domain. In comparison to analogue signal processing, this is more potent to system non-idealities, thereby requiring less calibration.

The design of a fully digital wideband receiver that produces targeted signal descriptor words requires careful consideration of two crucial parameters

- High input instantaneous bandwidth,
- High speed real-time signal processing.

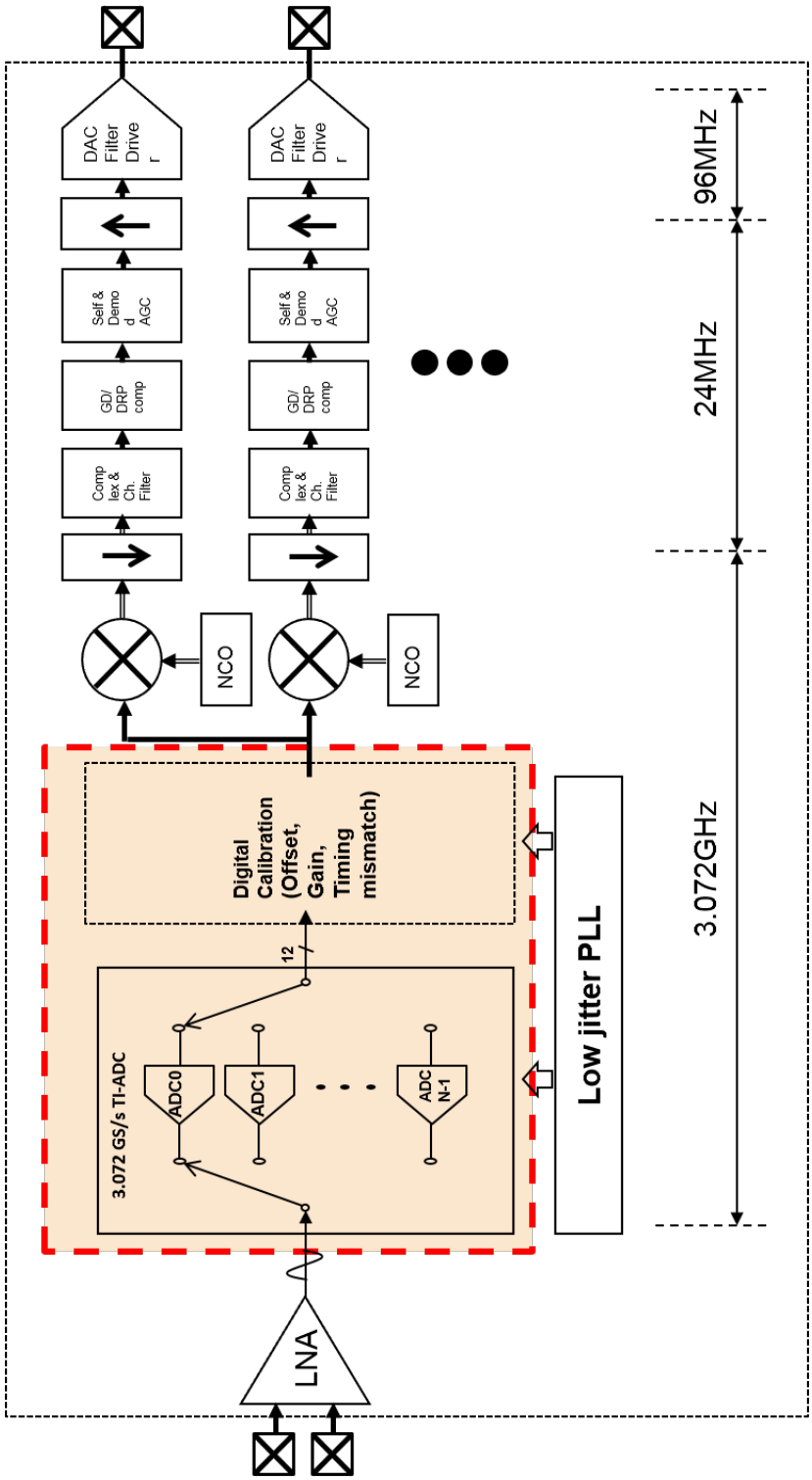


Figure 1: Wide-band Full Digital Receiver

Considering the major terrestrial digital TV standards such as Data over cable service interface specification (DOCSIS), Digial video broadcasting (DVB), and Advanced television system committee (ATSC), a digital wideband receiver must satisfy an operational frequency spectrum from approximately 40 MHz to 1 GHz [3] The structure of a wideband fully digital receiver is illustrated in Fig. 1. In accordance with the Nyquist criterion, a 1 GHz data signal will require a sampling frequency of more than 2 GHz for aliasing-free fair digitalisation. Thus, it is crucial to design an ADC that has a high sampling rate ($>$ 2 GHz), can operate in the wideband spectrum, and has high resolution, to minimise quantisation errors for accurate signal conversion.

The efficiency of a receiver can never outperform the efficiency of its ADC. At present, owing to the unavailability of credible ADCs with high resolution and the capability of simultaneously handling a wide frequency range, an alternate approach, using multiple bandpass filters in parallel, is used to extract the frequency of interest and then convert it to digital using low-speed (several MHz) ADCs [2, 3]. However, various issues are associated with such systems. The addition of extra circuitry makes them more complex in terms of implementation, resulting in noise performance degradation of the entire system. Frequency down-conversion requires a mixer and filter, and their parallel processing on parallel data streams, owing to which the circuit becomes bulky and more complex, resulting in high power and cost consumptions [3].

B. Contributions

This work focuses on designing a high-speed ADC that can provide higher accuracy, along with a larger, spurious-free dynamic range, while assuring lower

power consumption. Instead of using a single ultra-high-speed ADC, a parallel sampling approach is employed, in which multiple low data-rate ADCs are time-interleaved using phase-shifted sampling clocks to achieve a high overall sampling rate (GS/s). The resulting system can handle the complete operational frequency spectrum of major terrestrial digital TV standards, without the need for any additional down-conversion circuitry. The absence of mixers and filters results in lower complexity and power consumption. A 12 bit 3.072GS/s time-interleaved (TI) pipelined ADC is presented in this work. The proposed design is a heterogeneous unification of various high-performance components satisfying the Nyquist bandwidth requirements for any signal in the 1-GHz wide bandwidth. Relaxed implementation requirements are the key focus of this work.

C. Thesis Layout

The remainder of this thesis is organised as follows. Section 2 provides a brief review of the architectures and challenges associated with designing a Giga-sampling TI-ADC. Section 3 presents a comparison of existing clock-generation techniques and the structure of the proposed design, along with its benefits. Section 4 discusses the criteria of the sub-ADC selection for the TI-ADC, provides a brief introduction of the available techniques, as well as their pros and cons, and finally, describes the structure of the proposed technique and several important structures used therein. Section 5 discusses the structure of the proposed pipelined ADC and the design of its components. Section 6 deals with the sample-and-hold (S&H) circuit used in the TI structure. It discusses the structure of the amplifier-sharing technique employed in this design. Section 7 explains the effects of sequential interleaving on the performance of

the sub-ADCs and the designed fully digital background calibration technique implemented to deal with these. The results and measurements of the designed system and its comparison with other state-of-the-art designs are reported in section 8. Finally, section 9 concludes this thesis.

II. TIME-INTERLEAVED ADC OVERVIEW

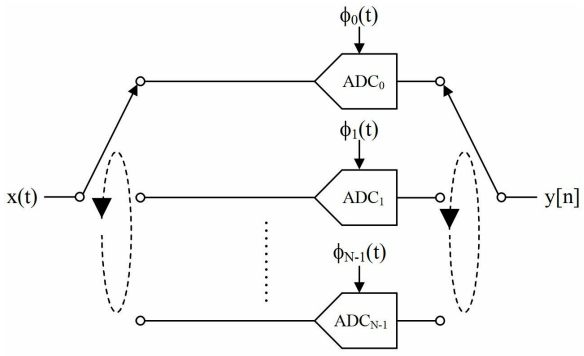
The TI-ADC is an *M*-channel architecture consisting of M number of ADCs with the same sampling speeds and different phase angles. The resulting system acts as a single ADC, the speed of which is *M* times that of an individual ADC [4]. The phenomenon of time interleaving itself is far more complex than simply placing sub-ACDs in parallel. Numerous repercussions, such as timing mismatch, offset error, and gain error, should be considered when designing a TI system. Moreover, the design of the S&H circuit for a TI-ADC is quite different from that of a non-interleaved ADC. In modern designs, a digital calibration block is usually employed to account for all mismatch calibrations.

Nonlinearities induced in TI-ADCs can be broadly classified as static and dynamic types. Compared to dynamic mismatch, static mismatch is substantially easier to deal with, as its effects are ideally independent of changes in the input frequency [5,6]. However, dynamic mismatches are significantly more responsive to frequency changes. Therefore, they are considered as the major contributor to limiting the spectral performance of the entire system. Fig. 2 illustrates the basic structure of the TI-ADC, with *x(t)* as input and *y[n]* as digital output. Considering the number N of sub-ADCs, with T_s being the sampling time for a single ADC, the sampling time of N sub-ADCs can be generalised as [7]

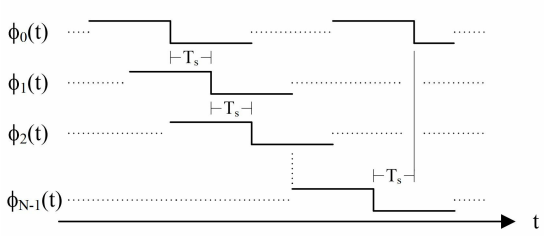
$$\widehat{T_S} = N.T_S \tag{1}$$

and the k^{th} sub-ADC will trigger at:

$$t_k[n] = n\widehat{T_s} + kT_s = (nN + k).T_s \tag{2}$$



(a)



(b)

Figure 2: (a) TI-ADC (b) sampling edges of sub-ADC clocks

Considering the input signal to be sampled uniformly (ideally), the output of the kth sub-ADC can be generalised as:

$$\widehat{Y}_k[n] = x(t_k[n]) = x([nN + K].T_s) \tag{3}$$

where *(n - k)/N* is an integer

$$Y_k[n] = \widehat{Y}_k\left[\frac{n-k}{N}\right] \tag{4}$$

The output from all of the ADCs is then multiplexed to achieve *Y[n]*, which is stated as:

$$Y[n] = \sum_{k=0}^{N-1} Y_k[n] \tag{5}$$

Moreover, *y[n]* can be further reduced as:

$$Y[n] = x(nT_s) \tag{6}$$

where *y[n]* is the output of the TI-ADC when all of the sampling periods are considered ideal. However, in practice, several mismatches such as gain, offset, and timing skew occur, which will affect the system performance. If the gain error of the ADC is G_k, the offset is O_k, and the timing skew is τ_k, eq. 6 can be generalised as:

$$Y_k[n] = G_k \cdot x(nT_s - \tau_k) + O_k \tag{7}$$

In the proposed design, 32 channels of the 12-bit 96 MS/s pipelined ADC are time-interleaved to achieve an overall bandwidth of 3.072 GS/s. Moreover, 32 non-overlapping clock phases are generated for synchronous interleaving of the sub-ADCs using the Johnson counter scheme. A fully digital background calibration block deals with the system nonlinearities. Details of all these components follow later in this literature.

III. CLOCK GENERATOR

Time interleaving requires sub-ADCs to operate on sampling clocks that have the same sampling speeds but different phase angles, such that only one of the *M* sub-ADCs is active at a given time. The generation of a precise clock phase for all channels is imperative to the system performance, as any skew in the generated phases can result in the sampling of incorrect values.

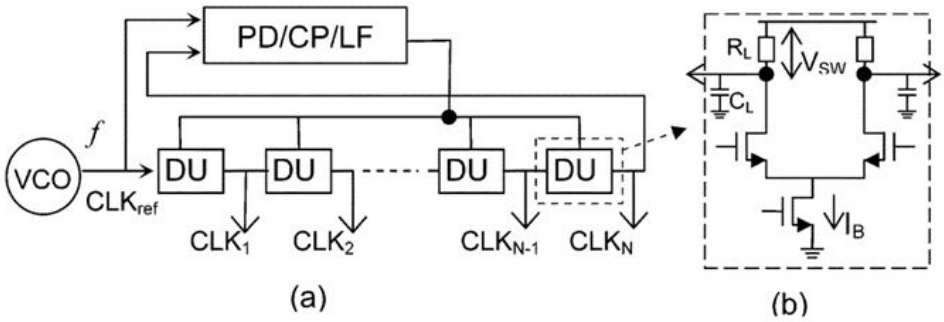


Figure 3: (a) DLL MPCG Structure (b) CML delay unit

Multiple techniques have been proposed for the generation of precise clock phases. However, aimed at multi-functionality, a multiphase clock generator (MPCG) that is flexible in terms of multiple data rates and radio frequencies was adopted [8]. Delay-locked loops (DLLs) and the shift register based MPCG are the two most widely used architectures. Fig. 3 shows the basic scheme of a DLL based clock generator. Compared to the DLL, an SR-based MPCG also provides the functionality of a divider for *N*-phase generation. Unlike DLLs, it requires an *N*-times higher clock to generate the *N*-clock phase. So, selection of clock generator is a tradeoff based on application requirement. However, SR MPCGs offer the advantage of no jitter accumulation from one stage to another, making

them a superior contender in a fair comparison. Other options include SR based synchronous clock divider as shown in Fig. 4, but it requires an injection locked oscillator. At higher frequencies it requires injection of input clock at multiple points in the loop to prevent jitter accumulation, thus SR based MPCG is a better alternative.

A. DLL Based MPCG

The structure of a DLL based MPCG consists of a voltage controlled delay line (VCDL), delay units and a control circuit. The control circuit has further 3 components, phase detector loop filter and a charge pump. Fig. 3a shows the architecture of a DLL based MPCG. First, a voltage controled oscillator (VCO) generates a reference clock CLK_{ref} with the target frequency f and propogates it through the voltage controlled delay line (VCDL). A phase detector then compares it with a previous output CLK_N of the VCDL and sends a control signal to the VCDL so that the delay time is one clock period of CLK_{ref}. In this way N clocks are generated with a phase difference of $2\pi/N$ between them.

Fig. 3b shows the structure of a current mode logic (CML) delay units. Owing to their low-supply noise and subtrate bounce rejection CML delay units are usually prefferd for designing DLLs. Due to the switching of the tail current the output voltage swing is decided by I_B and R_L. The delay of the delay unit can be determined by the RC network of R_L and C_L at the output nodes. The delay t_d of a CML delay unit with a diffential output swing V_{SW} can be approximted as [8]:

$$t_d = \ln 2 . R_L C_L \tag{8}$$

$$t_d = \ln 2 \cdot (V_{SW}/I_B) \cdot C_L \tag{9}$$

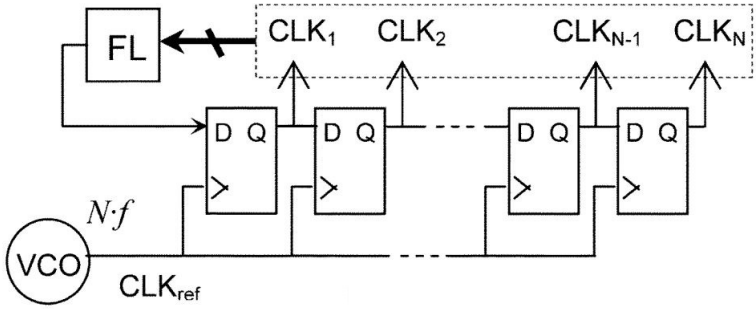


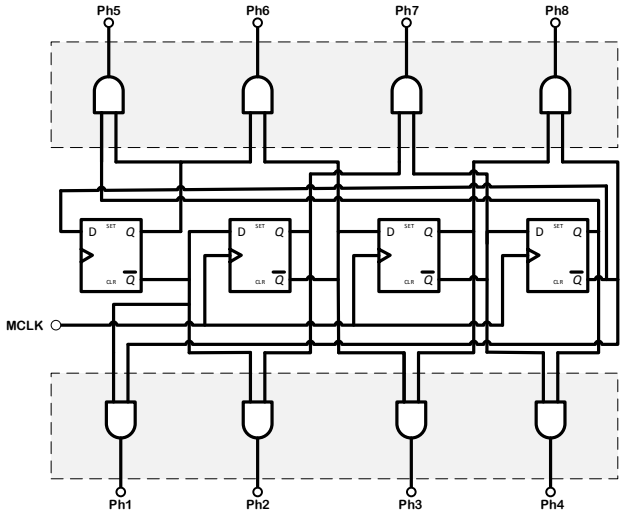
Figure 4: SR MPCG Structure

B. SR Based MPCG

Basic structure of a SR based MPCG is shown in Fig. 4. An SR-based MPCG is a chain of D flip-flops (DFFs) with N identical DFFs cascaded in series. A high-frequency reference clock generated from the phase-locked loop is fed to the DFF chain. A flip logic circuit continuously monitors the chain, and flips the value to the input of the first DFF following N reference clock cycles. As the DFFs are connected in series, the Q output of every DFF is delayed from its predecessor by one clock period of the reference clock. In this manner, N clock cycles with a phase difference of $2\pi/N$ are generated. The SR-based MPCG can be used in different topologies. This work, uses a modified Johnson counter-based approach.

1. Johnson Counter

The Johnson counter is a type of ring counter, also known as the twisted ring counter [9]. In this counter, N no. of DFFs are connected in serial chain (like in shift registers) and are clocked at same master clock.



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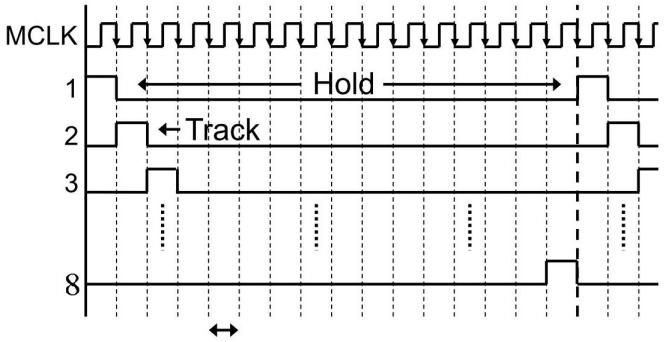


(b)

Figure 5: Proposed SR MPCG; (a) Modified Johnson Counter (b) Eight one pulse wide non-overlapping phase of master clock

Output of the first DFF is fed to the input of the next DFF, while the output of the last DFF in the chain comes to the first one. However, in contrast to a traditional ring counter, instead of Q the complement of the output Q' is sent to the input of the first DFF.

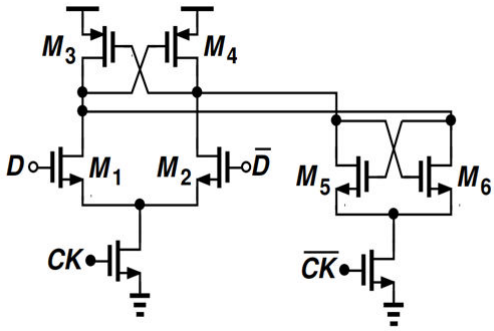


Figure 6: Current Mode Logic based D-latch

Thus, in Johnson counter the output of the first DFF changes state after every $2N$ no. of cycles, resulting in frequency of F_{mc}/N for each clock. Fig. 5 shows the structure of a Johnson and its waveform. As evident from the Fig. 5, unlike a traditional SR based MPGC topology, we get 8-phases from just 4 DFFs, by using there outputs along with there respective complements. Fig. 5b shows the Master Clock(MC) along with the shifted phases of sampling clocks. Each phase has equal track and hold period, and the sampling switch sequence is determined based on the phase. In order to increase the conversion time for the sub-ADCs and decrease the value of the input capacitance, a modified Johnson counter structure was implemented, as illustrated in Fig. 5a. Different combinations from the DFF outputs (Q and Q') were integrated using AND gates, such that each shifted phase tracks for only one clock period of the M_{CLK} and holds for the remaining N-1 cycles.

Different DFF circuit were tested in Johnson counter for accurate phase shifting at ultra-high speed. Firstly, a conventional approach in which two CML-based D-latches were used to construct a dynamic DFF, as shown in Fig. 6 was tested. But, due to the dynamic nature of this latches Q and Q' are not perfect

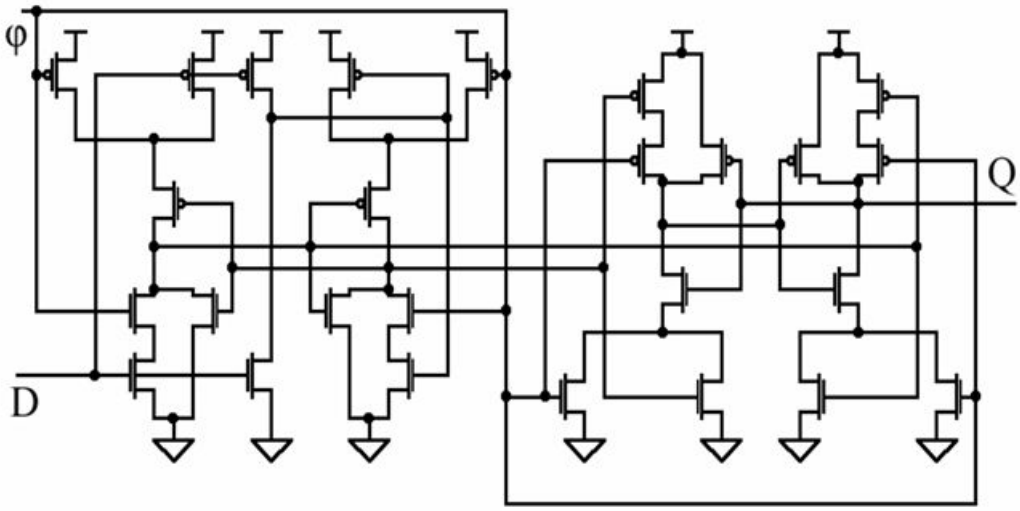


Figure 7: NAND-NOR master-slave flip-flop

compliments. Thus, they are not feasible for use in Johnson counter, as both the outputs of the DFF are used to generate clock phases.

Secondly, a NAND-NOR based master slave flip-flop was implemented as shown in Fig. 7. Design consists of a clock and two gated latches. Design has a better accuracy, but each latch required around 14 transistors, which resulted in high delays and high energy consumption per transition, which is not a preferred choice in a Time Interleaving system. Finally, a transmission-gate latch-based Master-Slave Flip-Flop was implemented. Fig. 8 shows a transmission gate (TG) latch-based Master-slave flip-flop. The traditional version of the circuit contains 3 TGs and 4 NOT gates. Based on the simulation results of all three topologies, it is evident that fine accuracy at high-speed and low power consumption characteristic of TG latch-based Master slave flip-flop makes them the most appropriate choice.

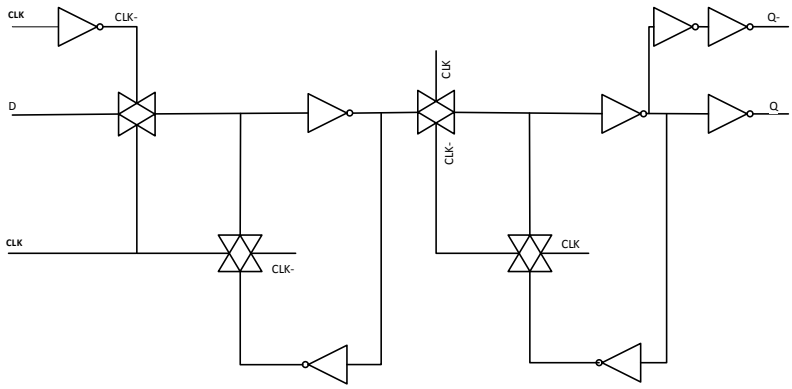


Figure 8: Transmission gate-based D-Flipflop

IV. CHOICE OF SUB-ADC

The conversion performance of a TI-ADC cannot surpass the performance of the sub-ADC used. Thus, the precise selection of a sub-ADC based on application is a formidable task. In the past decade, a remarkable advancement has occurred in ADC technologies. While there are ADCs operating at ultra-high frequencies (GHz), there are others that consuming ultra-low power (μW, nW). Every topology exhibit certain compromises among the sampling rate, resolution, power consumption, and other important performance indicators [10]. Therefore, selecting the optimal trade-off between different performance evaluators based on application is the key challenge in the selection of a sub-ADC. ADC applications can be broadly classified into four market segments:

- precision measurement
- data acquisition
- voice and audio applications
- high-speed applications

Most of these applications can be covered using sigma-delta (Σ-Δ), a successive approximation registered (SAR), Flash, and pipelined ADC. Fig. 9 illustrates the application segmentation of these ADCs with respect to their sampling speed and resolution. Although at varying instances the different ADC topologies overlap one another in terms of performance, the selection of architecture is based purely on the target application.

Flash ADCs are the fastest converters owing to their conversion topology, as they perform the conversion in a single step. However, they lose their significance

in high-resolution applications, because the circuit expands exponentially as the number of bits increases. Therefore, Flash ADCs are typically preferred for high-speed, low-resolution applications.

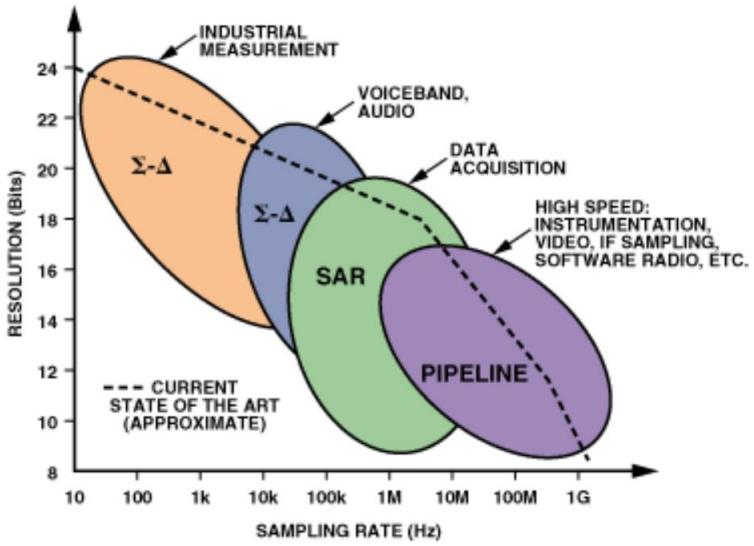


Figure 9: Market segmentation of ADC architecture (resolution VS sampling speed)

Sigma-delta ADCs are the preferred choice for high-precision applications. They use oversampling rates, decimation, and noise shaping to create an accurate digital representation of the analogue input signal. However, owing to the accumulation of bitstreams for longer periods, sigma-delta ADCs yield low effective conversion rates. Although they can be tuned for higher sampling rates, but they consume enormous amount of power for higher sampling frequencies. Therefore, their application is limited to the applications that requires low-medium speed with high resolution, high stability and low power consumption.

Successive-approximation analog-to-digital converters have emerged as the

most popular architecture in recent times. In addition to zero-cycle latency, low circuit latency, and high accuracy, they consume very low power and are due to simplicity of their structure they are quite easy to use. However, SAR ADC does the conversion step-by-step by implementing successive approximation to determine each bit. Due to the use of same architecture for each step, it requires a very high clock rate for the conversion to be completed before the next sample arrives. Consequently, SAR ADCs are low-speed converters and are preferred for the applications that require medium-high resolution with very low-power consumption capability.

Pipeline ADC another popular architecture for digitalizing circuits. Pipeline ADCs extends their capitalization from medium-high speed applications. In contrast to Flash ADCs, Pipeline ADCs consumes less power, and with the increase in resolution, structure expands linearly. But, due to the cascaded nature of the architecture, system suffers from data latency, but in most of the high-speed applications data latency is not an issue. Thus, Pipelined ADCs are the most preferred choice for high speed applications like instrumentation, video, radar and consumer electronics (enhanced definition TV, digital cameras). Although they replace Flash ADCs in most of high-speed applications, but low-resolution Flash ADCs still sustain their effectiveness as a major building block of Pipeline ADC.

In time-interleaved ADCs, as the no. of interleaving channels increases, mismatches like timing skew, bandwidth mismatch, offset error and gain mismatch gets intensified. Also, large no. of channels will result in a high-power consuming bulky structure. Increase in system non-linearities, will result in degradation of overall system performance. Therefore, it is necessary to choose an ADC, that has high-speed with an optimal compromise in power consumption

and accuracy. In addition to that, as we know, wide-band full-digital receiver has an operational frequency spectrum from 40MHz∼1GHz so it is important that the selected sub-ADC should have high input Nyquist bandwidth. Based on the above requirements, Pipelined ADC was selected as the sub-ADC in the proposed design.

V. PIPELINED ADC

As mentioned previously, due to their high-speed and low-power consumption (in comparison to other available high-speed architectures i.e. Flash ADCs) Pipelined ADCs are the most preferred choice for high speed applications. In addition to high-speed, with the increasing no. of bits their complexity increases linearly. The term "Pipelined" illustrates that the processing of the input signal is done cascaded in *n* stages. Fig. 10 shows the block diagram of Pipelined ADC.

In a pipelined ADC, each stage contributes a certain number of bits to the final converted output. The input signal enters the first stage, which resolves n bits, and then transfers an analogue residue to the next stage. The process continues until the signal reaches the final stage, following which an *m-bit* ADC (usually a low-resolution Flash ADC) resolves the final bits of the pipelined ADC.

$$x = Q_1 + \frac{1}{A_1}Q_2 + \frac{1}{A_1A_2}Q_3 + \frac{1}{A_1A_2A_3}Q_4 \tag{10}$$

Where Q is the quantisation output and A is the residue amplification gain. All of the stages in the pipeline pass their bits to the time alignment and error correction block, which time-aligns the output bits gathered at different time instances and performs necessary calibrations for error correction. The operation of a pipelined ADC is quite similar to that of a two-step Flash ADC. However, unlike a two-step Flash ADC, it does not need to wait for the residue to reach the end of the chain to conclude its bits. Once the residue is transferred to stage 2, stage 1 starts processing the next sample. In this manner, at any given time, all of the available stages in the pipeline are processing data, except at the beginning, where *n* clocks are required for the first sample to reach the end of the pipeline.

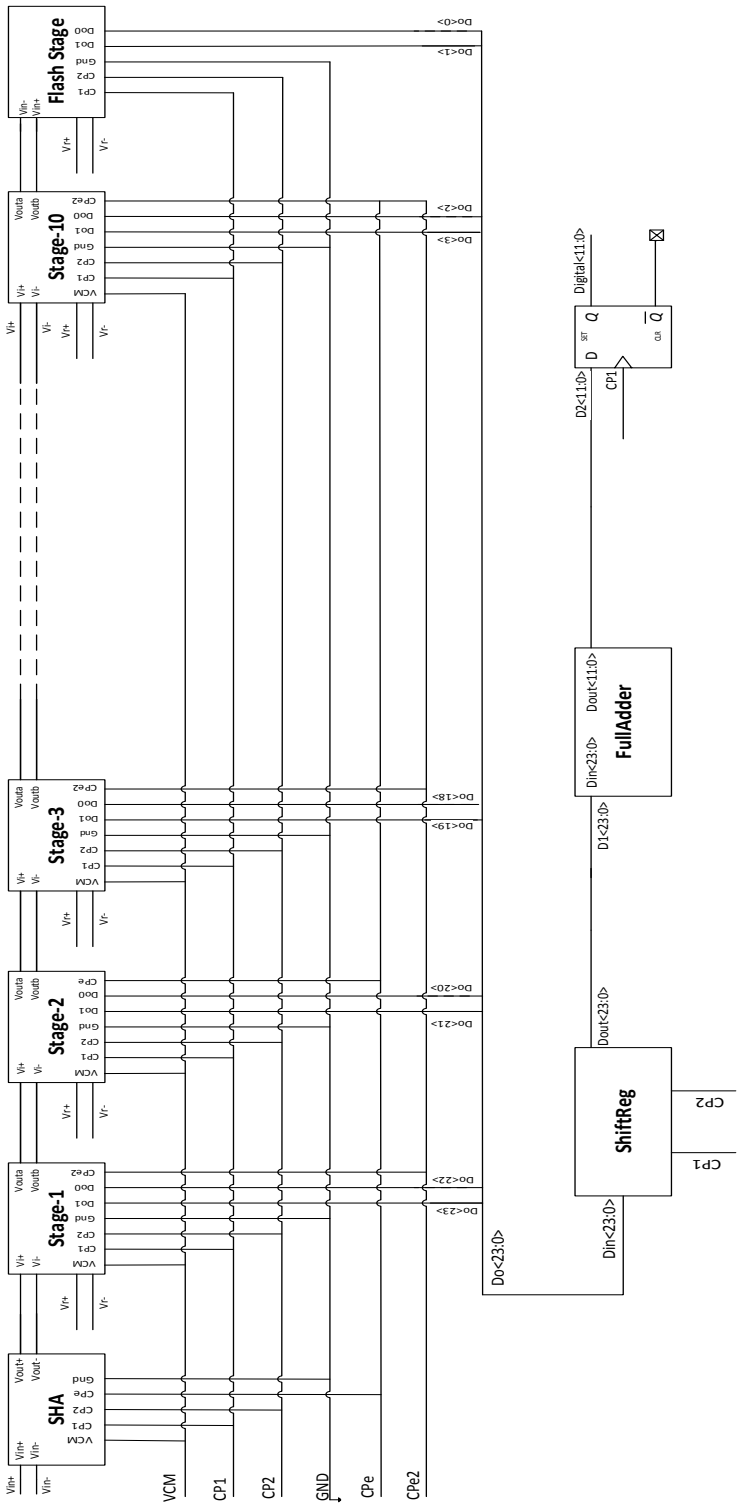


Figure 10: Proposed 12-bit Pipeline ADC block diagram

Thus, due to parallel processing of stages, Pipelined ADCs inhabit higher throughputs. The latency of the digital output depends on the number of stages in the pipeline: additional stages result in higher latency. The latency of the pipelined ADC can be minimised by increasing the number of bits per stage, but doing so will complicate the stage design requirements.

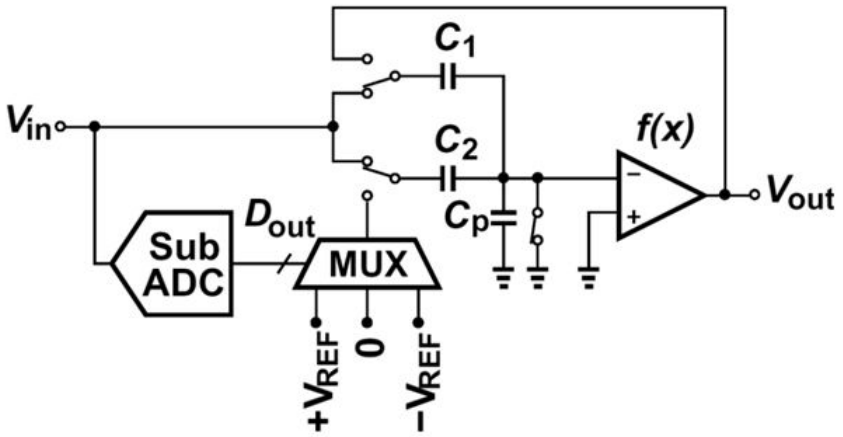


Figure 11: Block diagram of Pipeline-stage

Fig. 11 shows the structure of a single stage in pipelined ADC. Conventionally, pipeline-stage structure consisted of a Sample and hold (S/H), sub-ADC (usually Flash ADC), sub-DAC, summer and an amplifier. S/H block samples the input/residue signal, sub-ADC then quantizes the input sample and outputs n-bits. This signal is then converted back to analog by sub-DAC which is then subtracted from the input to generate residue. Residue is then amplified and passed on to the next stage for processing. However, in modern designs, sub-DAC, amplifier, subtractor and S/H for the next stage are summed up into a single block called Multiply-DAC (MDAC). Due to which the structure of pipeline stage shrinks down to a flash quantizer and a MDAC. Quantizer (sub-ADC) quantizes

the input/residue to generate n-bits, while MDAC accounts for residue generation, amplification and sampling.

Traditionally, all of the stages resolve the same number of bits per stage (except for the final stage). Generally, the number of bits per stage varies from 1 to 4 (with a redundancy of 0.5 bits for error correction). The most popular architecture among these is 1.5 bits per stage, the use of which simplifies the stage design requirements; that is, the requirement for a residue gain amplifier is $A_i = 2^n$ (where n is the number of bits per stage and i is the stage number) for the residue to acquire a full stage range for the approaching next stage [11]. However, with a 2^n amplification of the residue, any error in sub-ADC stage will lead to missing codes.

In order to account for the sensitivity of sub-ADC, 0.5-bit redundancy is employed to the stage structure. Instead of using $A_i = 2^n$ for full scale range, a half scale range with $A_i = 2^{n_i-1}$ is used for amplification, while the other half helps to accommodate sub-ADC errors. In addition to that, there is a one-bit overlap for digital correction between neighboring stages of the Pipeline, thus the total resolution of overall ADC can be stated as:

$$Resolution_{ADC} = No.of stages(n-1)+m \tag{11}$$

Where n is the no. of bits per stage, and m is the no. of bits in last ADC. Fig. 12 explains the pipeline redundancy scheme for a N-stage pipeline ADC. Because of this immunity to sub-ADC errors, pipelined ADCs are an attractive choice for high speed applications [12].

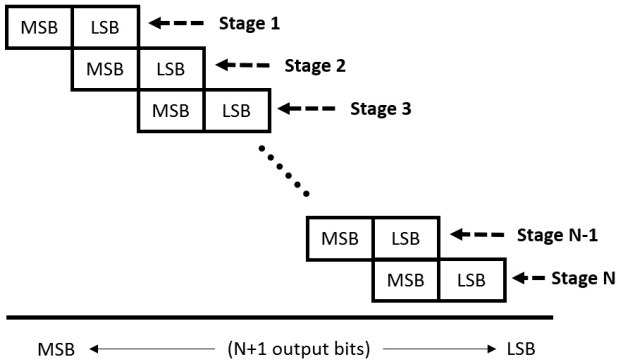


Figure 12: Redundancy scheme for N-stage pipeline ADC

When all of the bits are resolved, the digital error correction and time alignment block combines the bits from all of the stages, provides them with appropriate weighting, aligns them in time, and subtracts the redundant bits to attain target resolution.

While sub-ADC sensitivity is relaxed by redundancy in stage architecture, accuracy of MDAC structure is also crucial to the ADC performance. Especially, accuracy of MDAC in early stages is quite critical. An error produced in stage 1, will not just transfer down till the end of the chain, but also gets amplified on each step of the chain. Thus, resulting in non-linearity of the whole system. Most commonly, reason of performance degradation in MDACs is inter-stage gain error (IGE). When the gain of the amplifier is less than used in digital backend the slope of the residue will be less than the ideal value and the resulting output will lead to missing codes, causing severe degradation in SFDR and INL [12].

In order to decrease the number of stages and increase the ADC resolution, structures with different numbers of bits in the stages are designed. However, the use of different numbers of bits complicates the design requirements, while using the same number of bits per stage streamlines the design requirements for a

pipelined ADC. The same reference voltages can be used across the entire chain for quantizers and DAC circuits; the layout implementation is simplified and path mismatches are eliminated, decreasing parasitic capacitance. For this reason, the traditional 1.5-bit architecture is used in the proposed design. A total of 10 1.5-bit stages are cascaded with a 2-bit flash quantizer to achieve 12-bit resolution. A 1.5-bit architecture has two major parts: the sub-ADC (in the pipeline stage) and a MDAC. A detailed description and selected designs will follow later.

A. Comparator

The sub-ADC of the 1.5-bit stage is a simple 2-bit flash quantizer, consisting of two comparators and voltage references as shown in Fig. 13. In high-speed ADCs, the comparator design is highly critical to the overall system performance [13–15]. It is the main bottleneck in limiting the speed of a high-speed, high-resolution ADC. In the past decade, a remarkable advancement in comparator architectures has occurred, in terms of both speed and power consumption. Some of the stand-out candidates for high-speed applications include: the single-stage dynamic comparator [16], pre-amplifier-based latched comparator [17], two-stage dynamic regenerator comparator, and dual tail dual rail dynamic latched comparator [7]. Single-stage dynamic latched comparators offer the advantage of low power consumption, but owing to the capacitive paths from output nodes, they suffer from high kickback noise. Regenerative comparators and dual tail dual rail dynamic latched comparators are more stable, but exhibit the disadvantage of high offset in their outputs, making them a non-feasible solution for TI-ADC applications. In contrast, pre-amplifier-based latched comparators have high speeds, ensure low power consumption, and have a very low offset in

their outputs. Therefore, they are the most appropriate choice for our design as comparators are the major contributor to offset error in a TI-ADC system.

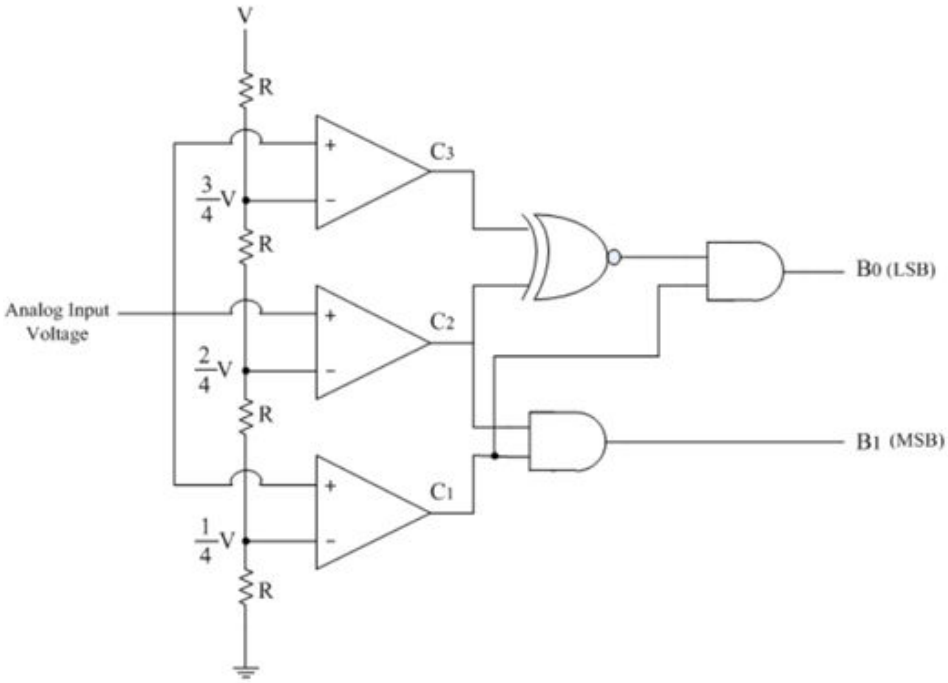


Figure 13: 2-bit flash quantizer (sub-ADC) used in pipeline stage

A pre-amplifier-based latched comparator completes conversion in three stages: pre-amplification, regenerative latch, and output latch. Fig. 14 illustrates the complete structure of the pre-amplifier-based latched comparator. There are two main advantages of using a pre-amplifier as the first stage. Firstly, it increases the conversion speed by amplifying the difference in the two signals, which reduces the comparison time for the regenerative latch. Secondly, it aids in reducing the offset error of the comparator [14]. For high-speed applications, it is necessary for the pre-amplifier to have higher values for gain and gain-

bandwidth (GBW), thus, multistage amplification is employed in the proposed design [15, 16]. The decision on the number of amplification stages is also crucial, as the system transmission delay also increases with the number of stages. The transmission delay of a pre-amplifier can be expressed as:

$$t = n\tau = \frac{n.A^{\frac{1}{n}}}{G.GBW} \tag{12}$$

where t is the transmission delay, n is the number of amplifiers, τ is the delay of each amplifier, A is the total gain of the pre-amplifier, G is the gain of the individual stage amplifiers, and GBW is the Giga-bandwidth of each stage. In the proposed design, a two-stage folded cascode amplifier is used for pre-amplification of the input signal. The circuit provides an effective gain of 58.98 dB, with a phase margin of 66.39°, and the effective GBW is approximately 1.602 GHz. The amplifier output is then passed on to the regenerative latch stage. The regenerative latch is considered as the decision-making stage of the comparator. Owing to its high speed, it is always a preferred choice in high-speed comparators. The clock-controlled structure consists of two cross-coupled pairs (one PMOS and the other NMOS) and positive feedback, which significantly enhances the comparator performance. The regenerative latch speed depends on the recovery time constant $\tau_{recovery}$ and the regeneration time constant τ_{regen}. Their values are:

$$\tau_{recovery} = 2R_{on,MN18}.C_{tot} \tag{13}$$

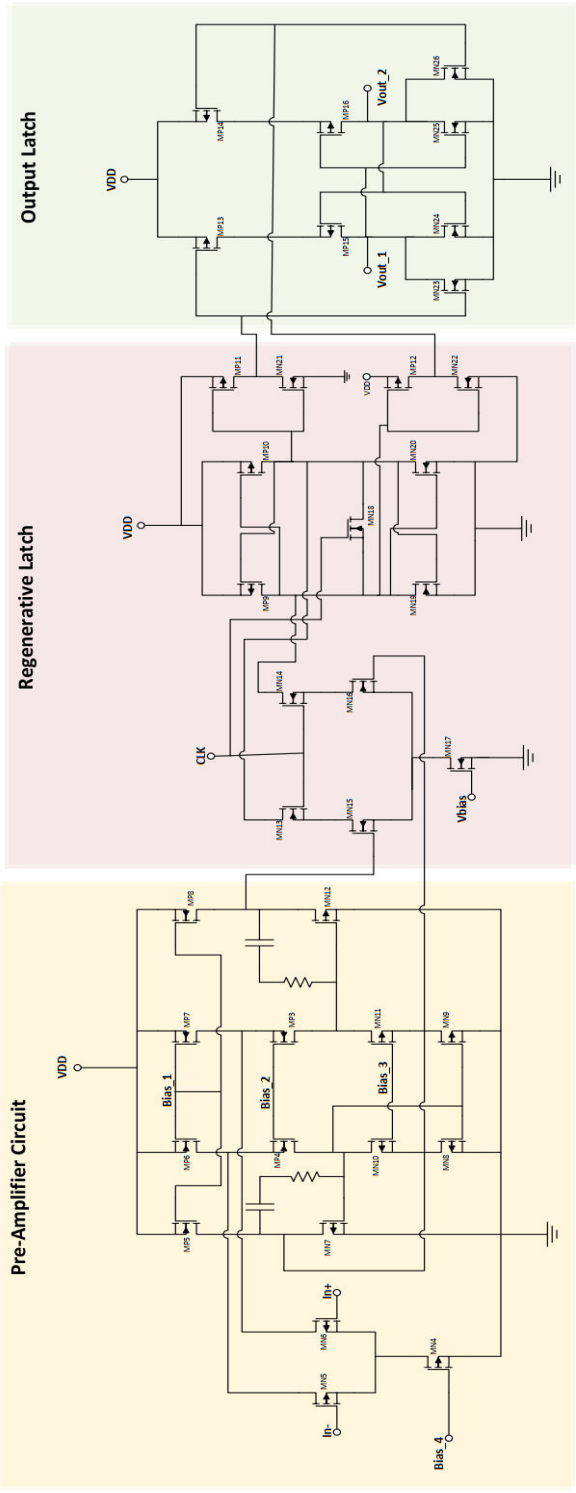


Figure 14: Pre-amplifier-based latched comparator

$$\tau_{regen} = \frac{C_{tot}}{g_{MP9,10} g_{MN19,20}} \tag{14}$$

Where $R_{on,MN18}$ is the on-time impedance of MN18, C_{tot} is the total parasitic capacitance, and $g_{MP9,10}$ and $g_{MN19,20}$ are the transconductances of MP9-MP10 and MN19-MN20, respectively. Thus, as is evident from Eq. 13, the recovery time of the regenerative latch can be decreased by decreasing $R_{on,MN18}$ (increasing the width of MN18). The regeneration time usually remains constant, because broadening the widths of MP9-MP10 and MN19-MN20 will indeed decrease $g_{MP9,10}$ and $g_{MN19,20}$, but it will increase the value of C_{tot} with the same ratio.

The final stage is an SR-latch that buffers the data at the output and keeps it stable. When the regenerative latch is in reset mode, the output latch will maintain the value of the last clock period, and it will only generate an output when the regenerative latch is in compare mode.

B. MDAC

The second most important block in a pipeline ADC is the MDAC, which is responsible for sampling the residue (from the previous stage), reconstructing the analogue equivalent of the digital output from the sub-ADC, generating the residue for the next stage by subtracting the reconstructed signal from the stage output, and performing and maintaining residue amplification. MDACs are switched capacitor circuits, and in the case of high-speed, high-resolution ADCs, the correct signal transmission to the next stage will depend on whether or not the MDAC is set up correctly. Therefore, designing an MDAC requires sophisticated consideration. Moreover, at present, devices operate on low voltages, which further complicates the MDAC design requirements.

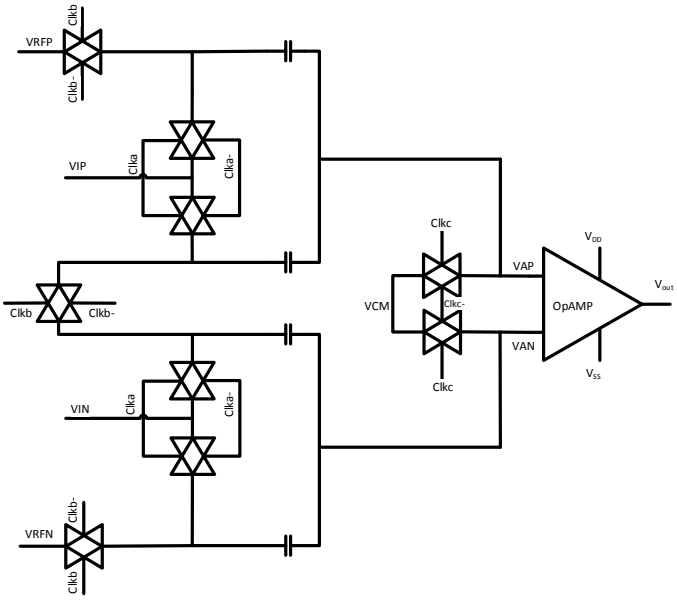


Figure 15: MDAC scheme used in 1.5-bit stage of Pipeline ADC

Structure of MDAC of a 1.5-bit stage is shown in Fig. 15, it consists of analog switches, sample/hold capacitances, operational amplifier and feedback capacitance.The circuit operates in two clock phases. In the first phase, the signal is sampled on the sampling capacitor, while the op-amp is in off mode, with its output connected to ground. In this case, C_s is the sampling capacitor and C_f is the feedback capacitor, and the charge on the capacitors can be expressed as:

$$Q_{C_s} = C_s V_{in}; \quad Q_{C_f} = C_f V_{in} \tag{15}$$

In the second phase, based on the values obtained from the sub-ADC, the associated reference levels are connected to the sampling capacitor (C_s), while the feedback capacitor (C_f) is connected to the operational amplifier output in a feedback configuration. In this manner, the difference between the sampled input

and DAC output is amplified by the charge transfer between the two capacitors.

A 3-to-1 multiplexer is used to switch among the three voltage levels $+V_{ref}$, *GND*, and $-V_{ref}$, and the decision is based on the digital bits received from the sub-ADC. If the digital output from the sub-ADC is 00, $-V_{ref}$ will be selected and the output of the 1.5-bit stage will be $2V_{in}+V_{ref}$; if the digital output is 01, *GND* will be selected and the output of the 1.5-bit stage will be $2V_{in}$; if the digital output is 10, $+V_{ref}$ will be selected, and the output of the 1.5-bit stage will be $2V_{in}-V_{ref}$.

As switched capacitor circuits, MDACs suffer from charge injection from the switches. Bottom plate sampling is employed, using it as an extra switch that shorts the input terminal of the operational amplifier during an extra phase that closes slightly earlier than phase 1. This results in a reduction of the signal-dependent offset and *on*-resistance of the sampling path, which decreases the bottom plate switch size.

As the decisive component in the 1.5-bit stage of a pipeline ADC, MDACs require meticulous analysis of the design parameters for the targeted performance. Op-amps are the most important performance indicator in an MDAC structure, and therefore it is of great importance that the *GBW* and gain of the op-amp should be sufficiently large, so that the residue signal can at least achieve the minimum amount of settling accuracy and can produce an output swing that is detectable by the succeeding stage. Moreover, in high-speed amplifiers, it is always desirable to use common-mode feedback for stable amplification. Furthermore, instead of using conventional CMOS switches (which lead to missing signals owing to their transmission characteristics), bootstrapped switching is used. The use of bootstrapped switches increases the *on*-conductance and linearity of the system and decreases the harmonic distortion,

leading to near-ideal switching performance.

1. Residue Amplifier

In high-speed, high-resolution ADCs, achieving the required performance in terms of the GBW, gain, noise, slew rate, and output swing within a limited power budget poses a significant challenge. The accuracy of an op-amp depends mainly on three factors: open-loop gain, capacitor matching, and settling time [12]. In new, scaled-down technologies, as the transistor size becomes smaller, systems are becoming prone to greater system non-idealities, thereby making it even more challenging to cope with the higher performance requirements.

It is well known that, in pipelined ADCs, op-amps transfer finite gain error to their succeeding stage. In order to achieve the accuracy requirements of an n-bit pipeline ADC, it is imperative that this error should be less than the *LSB* voltage of an ADC with $(n - m)$ bits resolution, where m is the number of bits in each stage and n is the total resolution of the pipeline ADC [18].Thus, to satisfy the accuracy requirements, all stages should comply with:

$$\left(\frac{1}{\beta} - \frac{A}{1+A\beta}\right)\frac{V_{ref}}{2^m} \leq \frac{V_{ref}}{2^{n-m}} \tag{16}$$

Where A is the total amplifier gain and β is the inter-stage gain factor. In the proposed design, $n = 12$ bits and $m = 2$ bits, and thus the minimum required open-loop gain of the amplifier is 72.25 dB. To account for process variations in submicron technologies, it is preferred to have a gain that is higher than the required value, which also aids in minimising gain and offset errors.

The second most important parameter of this design is the *GBW* product of the amplifier. In order to attain the required accuracy, the *GBW* should be

substantially larger than the sampling frequency. As with gain requirements, the error produced by the minimum *GBW* should also be less than *1-LSB* of an ADC. Therefore, all stages should comply with:

$$GBW_{single-p} = \frac{(n-m+1)\ln 2}{2\pi.\beta.T_{set}} \tag{17}$$

As the sampling clock of the proposed pipeline ADC is around 100 MHz, in keeping with a conservative estimation, the settling time (T_{set}) of the system should be approximately 3 ns. Thus, the minimum required $GBW_{single-p}$ calculated from Eq. 17 is 809 MHz. For a two-pole feedback system, $GBW > 2GBW_{single-p}$, thus, the required *GBW* is approximately 1.62 GHz.

To satisfy the gain and *GBW* requirements, a gain-boosting technique was employed in the designed op-amp structure. The target was to increase the op-amp gain without affecting its output swing. The proposed design performs amplification in two stages. Based on the high-gain, high-bandwidth requirement, a folded cascode topology was selected for the first stage, while the second stage is a simple common emitter amplifier. The gain provided by the folded cascode stage can be estimated as $\frac{(g_m r_{out})^2}{4}$, while the gain produced by the second stage can be stated as $\frac{g_m r_{out}}{2}$. Thus, the total gain of the amplifier becomes $\frac{(g_m r_{out})^3}{8}$.

Fig. 16 illustrates the circuit of the proposed amplifier and its associated designs. Using the CM (Common Mode) voltage generator for the amplifier, the CM voltage can be adjusted by varying the value of VDD_{mid} to stabilise the static operating point at the output. As the transfer function of the system has two poles (for two stages), hand-designed compensation was implemented using C_c and R_c. Initially, the value of the compensation capacitor C_c was evaluated as *1 pf*, but in order to attain an improved phase margin, the value was further adjusted to

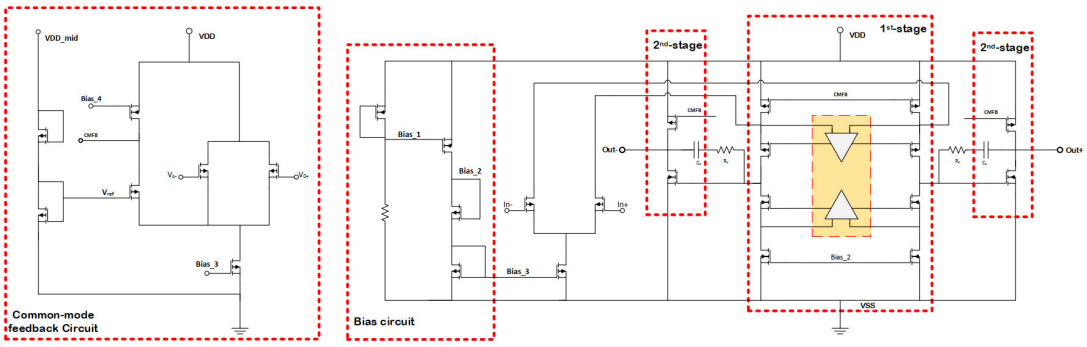


Figure 16: Two-stage folded cascode high-performance amplifier

880fF after repeated simulations, and the value of R_c was evaluated as 100 Ω for the desired compensation.

As a result of the hand-designed calibration components, the phase margin value is slightly overrated, but provided that the settling time requirements are met, the circuit will remain stable.

C. Bootstrap Switch

MDACs are switch capacitor structures, ideally switch should have '0' voltage drop across it. And, in order to avoid harmonic distortions on-resistance of the switch should also remain constant. However, modern nanometer switches suffer from a series of non-idealities. Due to which degradation in mobility of the channel causes on-resistance of the switch to vary with the change in input. On-resistance of R_{on} of a CMOS switch can be given as:

$$R_{on} = \frac{1}{\mu C_{ox}(\frac{W}{L})(V_{DD} - V_{th})} \tag{18}$$

Where C_{ox} is oxide capacitance and μ is mobility of electrons. Nanometer MOS-switches also suffer from inversion layer charge accumulation, a portion

of which is injected to the sampling capacitance, which causes errors in sampled signal. Total charge accumulation in the inversion layer can be expressed as:

$$Q_{IL} = W.L.C_{ox}\,(V_{DD} - V_{in} - V_{th}) \tag{19}$$

In order to have high linearity in high-resolution bootstrapping is used. Bootstrap circuit pumps up the voltage to force the switch to work in deep triode region. When the clock is high S_1, S_3 and S_4 are on, the gate of M_1 is grounded and VDD is applied across capacitor C. When the clock gets low, S_2 and S_5 are on, now the charged capacitor is connected between the gate of M_1 and the input V_{in} providing a constant DC voltage. Due to which the on-resistance R_{on} of the switch remains independent of the change in input voltage, resulting in high-linearity.

In proposed design, first half of the circuit is a voltage multiplier structure that acts as a charge pump increasing the voltage to approximately twice the supply voltage at the gate of M_3, thus charging C_3 to VDD while the phase is high. In the second half of the circuit M_7, M_8, M_{10} are used to enhance the gate voltage of M_9, turning it off completely, while the phase is low. Thus, the switch acts as a near ideal switch even on high-sampling rates.

D. Digital Error Correction and Time Alignment

To reduce the sensitivity of comparator redundancy is employed by introducing extra-bits. This stage combines the bits from all the stages, provides them proper weighting, align them in time and subtracts the redundancy bits to attain target specification. This block can be divided into two portions:

- Time alignment logic.

- Digital correction Logic.

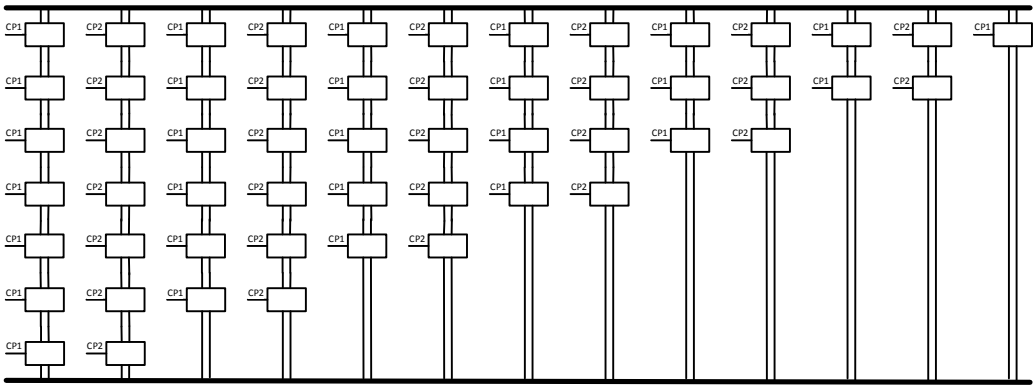


Figure 17: Time-Alignment configuration for bits arriving at different intervals of time in a 12-bit Pipeline ADC

As we know that in a pipelined ADCs, different bits are resolved at different instance of time. Therefore time-synchronization is required to combine the bits arriving at different clocks into a single word. In a pipeline ADC when the sampled signal is converted to digital bits by the sub-ADC, the output needs to be stored somewhere until the last stage has processed the residue. The logic is mainly composed of flip-flops or shift registers, which phase shifts the digital bits to make them arrive at the same time. Fig. 17 shows the structure of time alignment block. Digital value from the sub-ADC is stored in the first flipflop. On every transition in clock, digital value is passed down on to the next flipflop in cascode, until it reaches the last flipflop in the chain.

Once all the bits are time aligned, digital correction logic is applied to eliminate system non-linearities and quantization errors. The use of redundancy relaxes quantization specification. These redundancy bits are used for correction

of non-idealities and get eliminated in digital correction logic. Digital correction logic used in 1.5-bit stage structure of the proposed design has an actual resolution of 1-bit while the remaining 0.5-bit are there to provide redundancy.

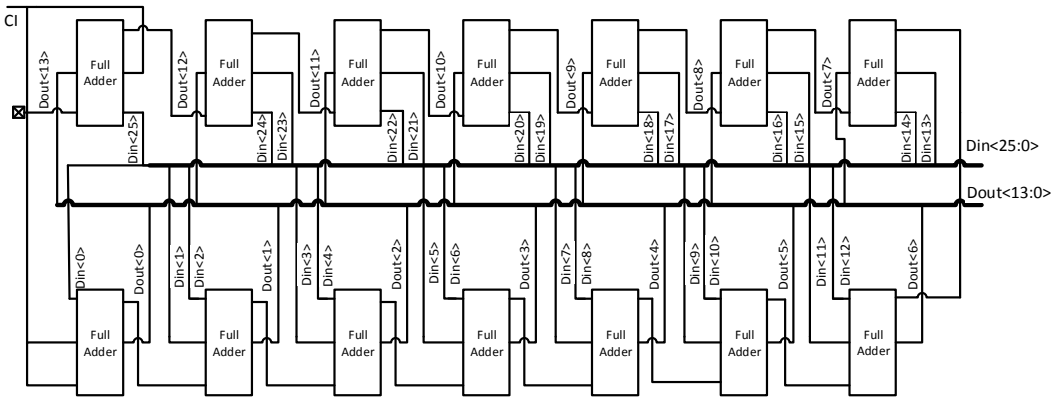


Figure 18: Digital error correction logic of 12-bit Pipeline ADC

S1	0	0										
S2		1	0									
S3			0	1								
S4				1	0							
S5					1	1						
S6						1	0					
S7							0	1				
S8								1	1			
S9									0	0		
S10										0	1	
S11											1	0
=	0	1	0	1	1	1	0	1	1	0	1	0

Figure 19: Digital correction logic scheme

There are 3 possible digital outputs of a 1.5-bit structure 00, 10, 01. 00 and 10 perfect decision (positive or negative) while 01s are non-decisive outputs. These digital outputs are sent to the DAC and the digital error correction. DAC generates the residue based on these bits (with error) and pass it on to the next stage,

these errors are then resolved by the digital correction logic. Structure of digital correction logic is shown in Fig. 18. The structure consists of Full-Adder circuits, each adder takes its decision based on 2-bits input from the respective stage, and a carry bit from the preceding stage. The operation of digital correction logic is shown in Fig. 19 for better understanding. Some modern designs also incorporate a digital output buffer along with time alignment and correction blocks. In the proposed design, considering space and power constraints output buffer was not included.

VI. SAMPLE AND HOLD CIRCUIT

In high-input frequency and high-sampling circuits sample and hold circuits are considered as a core necessity. Although there are structures without a SHA-block which provides the advantage of low power consumption, but they don't count for the timing skew between the passive switched capacitor and the sampler circuit and the sub-ADC, which ultimately leads to system performance degradation. Precision of sample and hold circuit is very important in a Time-Interleaved structure, as it deals directly with a continuous time signal and any error produced due to deviation in sampling moment will flow down the circuit.

There are three popular topologies of sample and hold circuit for time-Interleaved ADCs. First one is S/H without a front-end sampler. In this topology, each channel has a separate S/H structure. On each clock cycle one of the ADC goes from track to hold capturing a sample of the input signal. The disadvantage of this structure is that, the input capacitance of the TI-ADC gets very large, which limits the bandwidth of the system. Second type is S/H with a front-end sampler. In this topology, front-end sampler determines all the sampling instances due to which there is no timing misalignment between the channels of the time interleaved ADC. But in this structure, the track time of each channel cannot exceed half clock-cycle because the front-end operates at full sample-rate. Third type is hierarchical front-end sampler. In this technique large capacitance due to wire and switches is avoided by using a hierarchy S/H sampler. In each stage of hierarchy only one switch is on at a time. A channel will not start unless all the S/H switches in its chain are on. Although this technique provides better time alignment, but it introduces bandwidth mismatch between the channels which limit the performance of the converter.

In proposed design, a simple S/H without a front-end topology is used. By decreasing the track time of the sampling signals, high input capacitance issue was resolved. Small track time requires smaller capacitances, which results in an overall small input capacitance. Design uses an amplifier sharing scheme, in which an operational amplifier is shared between two channels. The circuit utilizes the idle time of the op-amp. circuit, resulting in low power and area consumption as the no. of op-amps is reduced from *M* to *M/2* (where *M* is the no. of channels in TI-ADC) [19].

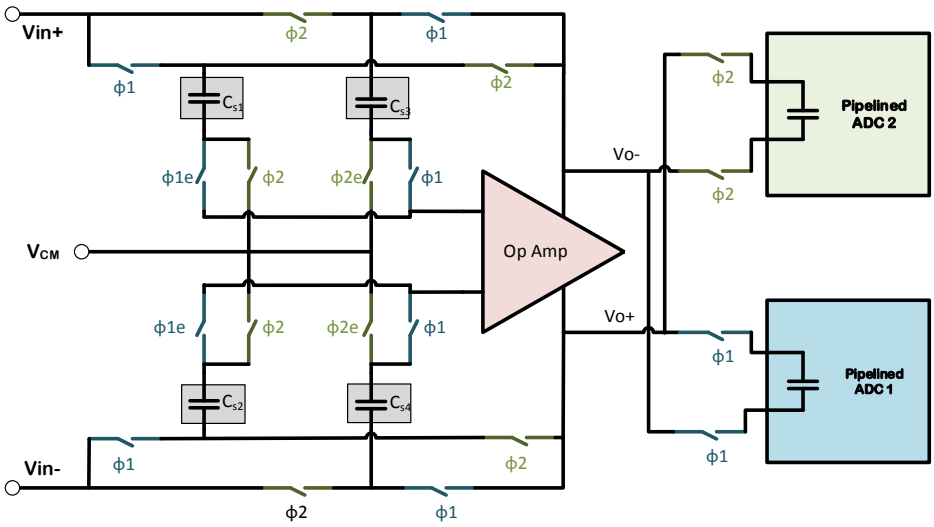


Figure 20: Amplifier-sharing S/H architecture used in TI-ADC

Fig. 20 shows the op-amp sharing configuration used in proposed design for two channels. When ϕ_1 is high the S/H circuit is connected to ADC_1, C_{S1} is connected to V_{cm}, C_{S2} is connected to the differential inputs, C_{S3} and C_{S4} are connected in feedback and V_{O+} and V_{O-} are connected to the sampling capacitor of ADC_1. When ϕ_2 is high, S/H gets connected to ADC_2, C_{S2} is connected to

V_{cm}, C_{S1} is connected to the differential inputs, C_{S3} and C_{S4} are connected in feedback and V_{O+} and V_{O-} are connected to the sampling capacitor of ADC_2. The configuration may cause systematic common mode errors, but the pipeline stage ahead of this block is fully differential thus no error is passed on the circuit. In order to assure overall stability of the system gain and GBW of the op-amp used in S/H block should be same as in the pipeline circuit proceeding it. Thus, same amplifier structure was utilized for op-amp in the sample and hold circuit.

VII. DIGITAL BACKGROUND CALIBRATION

In an ideal scenario, an M-channel TI-ADC should have the same gain, bandwidth, and sampling time for all sub-ADCs, but in practical scenarios, this is not possible, owing to component variations. Thus, the system is exposed to a series of mismatches that result in system performance degradation. Both analogue and digital solutions to this problem exist, but analogue solutions are more prone to thermal noise, voltage changes, and temperature variations, so digital solutions are preferred [20, 21].

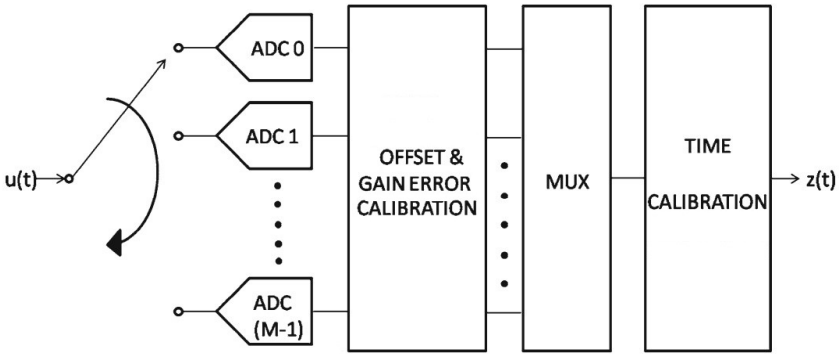


Figure 21: Digital background calibration scheme

Three main types of mismatches may appear in the TI-ADC: offset, gain, and time skew. Various calibration techniques have been proposed to address these issues. In this design, an autocorrelation-based background calibration technique is used for offset and gain calibration. The method employs the statistical signal properties, where the mean of the signal is used to estimate errors. The offset and

gain calibrated signal is then calibrated for the timing skew, using a register-controlled DLL-based timing calibration scheme. Fig. 21 presents the block diagram of the proposed calibration technique.

A. Offset and Gain Calibration

Ideally, without any mismatch, the overall average of n samples of the input signals in any given channel should be similar to all other channels, namely $x_0(n) = x_0(n) = x_1(n) = ... = x_M(n)$, which, in an ideal scenario, should be equal to the mean of the input (which is 0). In this method, we take a reference output and then compare all other outputs with the selected reference. The reference is estimated by taking the mean value of all samples from all channels.

$$x_{0,ref} = \sum_{i=0}^{N*n-1} u_i \tag{20}$$

For a more precise reference, the difference between the total average reference and individual average of each channel is calculated, which provides the deviation of offset error in each channel, $x_{0,ch(M)}$. The difference between the reference channel average and individual channel average is the corresponding offset error e_0 of that channel.

$$e_0 = x_{0,ch(M)} - x_{0,ref} \tag{21}$$

Thus, the offset corrected channel can be expressed as:

$$x_{0,corr(M)}(n) = x_M(n) - e_0 \tag{22}$$

Similar to the offset, with no mismatch, all of the channels should ideally produce the same signal power. If a mismatch exists in the channel powers, it

will cause a mismatch in the offset corrected outputs of the TI-ADC. The gain error is calibrated in the same manner as the offset error, except that, in the gain error calibration, the reference signal is the average of the squared offset corrected M-channel sample values (n). The outputs of all channels are compared with the reference channel. It is well known that the gain errors are multiplied into the input samples, so instead of subtracting (as in offset calibration), calibration is conducted by dividing the channel values by the calculated reference values.

$$e_{g(M)} = \frac{x_{g,ch(M)}}{x_{g,ref}} \tag{23}$$

Thus, the gain corrected outputs will be:

$$x_{g,corr(M)}(n) = \frac{x_{o,M(n)}}{e_{g,(M)}} \tag{24}$$

B. Time Skew Calibration

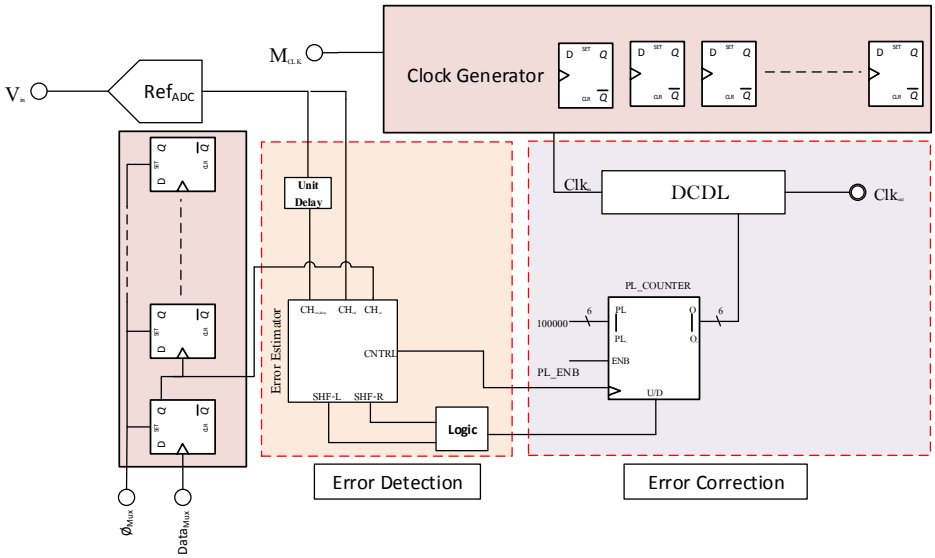
Owing to its frequency-dependent characteristics, time skew calibration requires significant attention. Unlike offset and gain mismatches, for which the power tones remain constant, the time skew is influenced by changes in the input frequency and conversion rate. Moreover, in high-speed circuits, in which input undergoes fast transitions, timing skews may cause even larger sampling errors. Therefore, for a wideband system, time skew calibration requires thorough consideration.

Despite its advantages, the autocorrelation-based calibration technique proposed in [21] imposes a strict restriction on the input statistics. The sign-equality-based background timing skew calibration proposed in [22] provides immunity against the varying input statistics, along with lower hardware

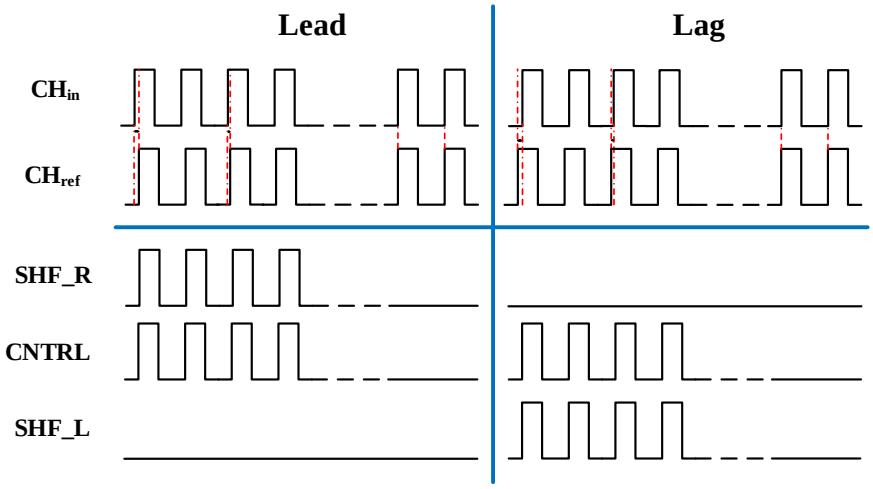
overheads, but the offset and initial timing mismatches degrade the calibration accuracy. A register-controlled DLL-based calibration scheme is proposed in this work. In addition to addressing the above issues, the proposed algorithm provides accurate time skew calibration.

The offset and gain calibrated signals from all of the channels are combined using a multiplexer. To calibrate the system time skew, time error estimation is required, for which the estimation of the input and its first derivative is necessary. In the proposed design, timing mismatch alignment is conducted in two parts. In the first part, the derivative is estimated by introducing a delayed version of the input channels and then comparing the difference with the reference ADC channel output. However, the exact value of the derivative is not required, as it only needs to indicate whether the input signal is leading or lagging the reference signal. On this basis, the direction of calibration will be decided. In the second part, based on the output from the error estimation block, an up/down counter will set its count direction. The output of this counter is connected to binary-weighted digitally controlled delay lines. Based on the counter value, the digitally controlled delay lines will delay the input signal by a certain value.

Fig. 22a illustrates a block diagram of the proposed timing calibration scheme. The multiplexer output enters the timing calibration block. The channel to be calibrated, CH_{in}, is extracted from the multiplexer output using a chain of DFFs. A reference signal CH_{ref} from the output of the reference ADC is fed into the unit delay block, which produces a delay version of the reference signal. Two signals, CH_{in} and CH_{ref}, enter the error estimation block, where the relative timing of the two signals is compared. If the input signal is lagging the delayed feedback signal, the shift-right will be high, while if the input signal is leading the delayed feedback signal, the shift-left will be high [20].



(a)



(b)

Figure 22: (a) Register-controlled DLL-based timing skew background calibration scheme. (b) waveforms of error-detection blocks.

The third output *CNTRL* is high when either the shift-right or shift-left outputs are high. This serves as an enabling signal for the counter in the error correction block.

A six-bit asynchronous parallel load counter is used in the error correction block. To decrease the convergence time, parallel load input is used to load 100,000 (mid-value) into the counter at the circuit start. When the *CNTRL* output becomes high, the counter is enabled. The counter direction is decided by the *SHF-L* and *SHF-R* outputs; a control logic circuit sets the counter to count *UP* if the *SHF-R* is high, and *DOWN* if the *SHF-L* is high. The resulting counter output is then connected to a binary-weighted digitally controlled delay line, which delays Clk_in by a certain amount based on the value from the counter. The cycle continues until the rising edge of the input clock CH_{in} is within the rising edge of the feedback clock CH_{ref} and its unit delayed version. All the outputs of the error detection block, namely *SHF-R, SHF-L*, and *CNTRL*, become low and the delay is locked.

In order to provide enough time for DFFs to operate and the generated output to get stable, the phase detector was operated at $a/2$ rate, due to which phase detector waits for around 2-cycles between two decision. Doing so indeed increases the training time of the ADC, but it provides better stability to the Phase Detection Circuit.

Another crucial point for the power efficiency of the TI-ADC is the resolution of the reference ADC. Since the reference ADC will be operating at the full clock frequency of the TI-ADC, flash-ADC was chosen as the reference ADC, considering its highspeed capabilities. As we know that the correlation of the sub-ADC with the reference ADC does not require accurate digitalization of the signal by reference ADC instead a noisy signal can be used for estimating the

timing skew. Therefore, it is possible to reduce the resolution of the reference ADC to single bit. However, using lower resolution for the reference ADC will result in increasing the training time of the TI-ADC. On the other hand, the power consumption will increase exponentially with the increasing resolution of the reference ADC. Therefore, considering both concerns, a flash ADC with an optimum resolution of 4-bits was selected as the reference ADC.

VIII. MEASUREMENT RESULTS

The proposed design was implemented in the Samsung 65-nm CMOS process. The performance was verified for both the static and dynamic parameters. The proposed ADC design was clocked at 3.072 GHz and powered with a 1.2V digital supply and 1.8V analog supply. The performance of TI-ADC cannot surpass the performance of sub-ADC, therefore seperate testbenches were created for critical components.

Generation of accurate clock phases for a formidable challenge, different D-Flipflop structures were implemented and tested to generate precise clock phase to decrease the timing skew of the system. All architectures were tested with the same clock of time-period of 0.3ns, pulse width is 0.15ns and state transition time 10ps. A random bit-stream was attached to the system with a time-period of 2ns and pulse width of 1ns. Fig. 23 is the output of a Current Mode logic-based D-latch circuit. The circuit laches the input value fine but there was high distortion in both the outputs Q and Q'. The distortion gets worse as we move towards higher frequencies and the state transition time of the circuit increases. Fig. 24 is the output of a typical master-slave D-flipflop architecture. Output indicated that the circuit has a faster state transition time and less distortion in the outputs in comparison to CML based D-Latch. But when the scheme was applied in a SR chain, adjacent phases showed overlapping at a longer range of time. The adopted scheme for this project is a true single pulse clock (TSPC) based D-flipflop. The traditional architecture of a TSPC based D-flipflop was modified to get Q' for its use in Johnson's counter (as Johnson's counter used both the outputs of DFF).

Fig. 25 shows that the output of this architecture has the least distortion in comparison to other implemented schemes, state transition time is low, in

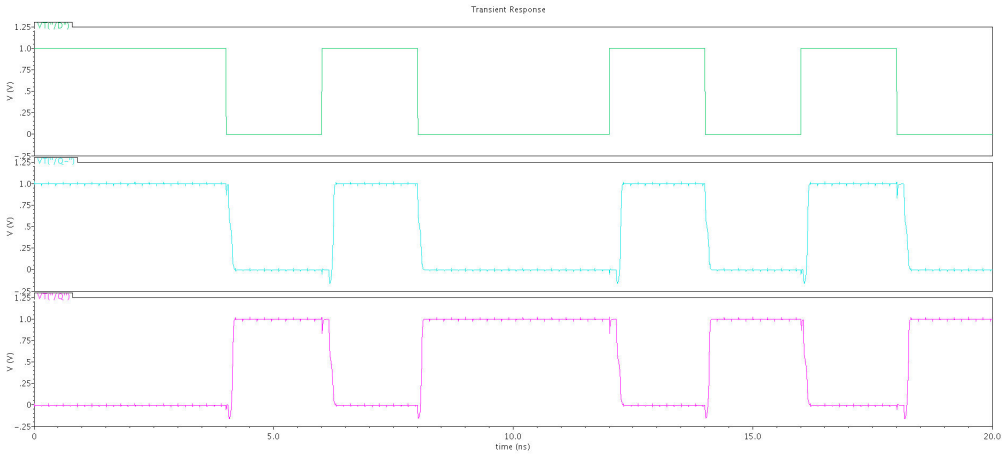


Figure 23: CML based DFF

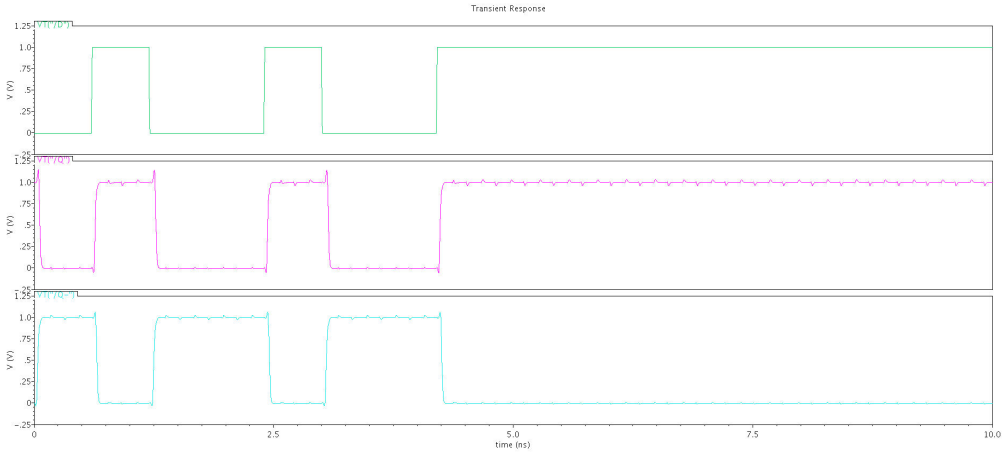


Figure 24: Master-slave DFF

addition, circuit consumes less power then other as the conversion completes in a single cycle. Although there was a small starting offset in the modified design, but it won't be a problem for our desired application, as all the generated phases will have the same amount of offset and there will be no overlapping among the adjacent phases.

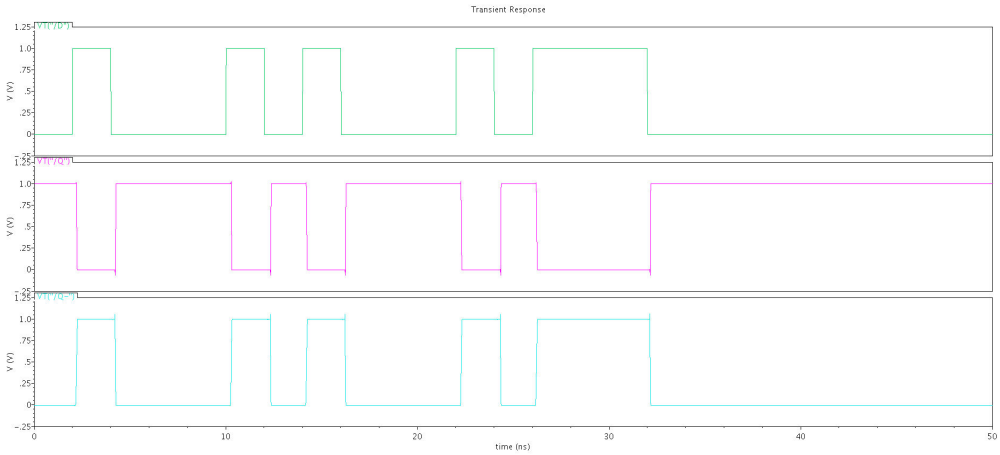


Figure 25: TSPC based DFF

Johnson counter scheme was used for the generation of non. overlapping phases. Performance of the design was tested by generating 8 non-overlapping phases form 4 TSPC D-flipflops. Each D-flipflop was clocked at the master clock, with a time-period of 0.3ns, pulse width is 0.15ns and state transition time of 10ps. Fig. 26 shows the output of the Johnson's counter. On each positive edge of the master clock one of the 8-phases goes from low to high. All the phases are equal with a time-period of 2.4ns and the pulse width of 1.2ns. Each phase repeats itself after eight pulses of the master clock and changes its state (from high to low) after every four pulses of the master clock.

Johnson's counter circuit was further modified by introducing two reference clocks +ref and -ref to ensure that there is no overlapping among the clock phases. Each reference clock has half the frequency to the master clock and are 180° out-of-phase to each other. Time period of the reference clock is 0.6ns and pulse width is 0.3ns. Fig. 27 shows the output of the modified clock generator.

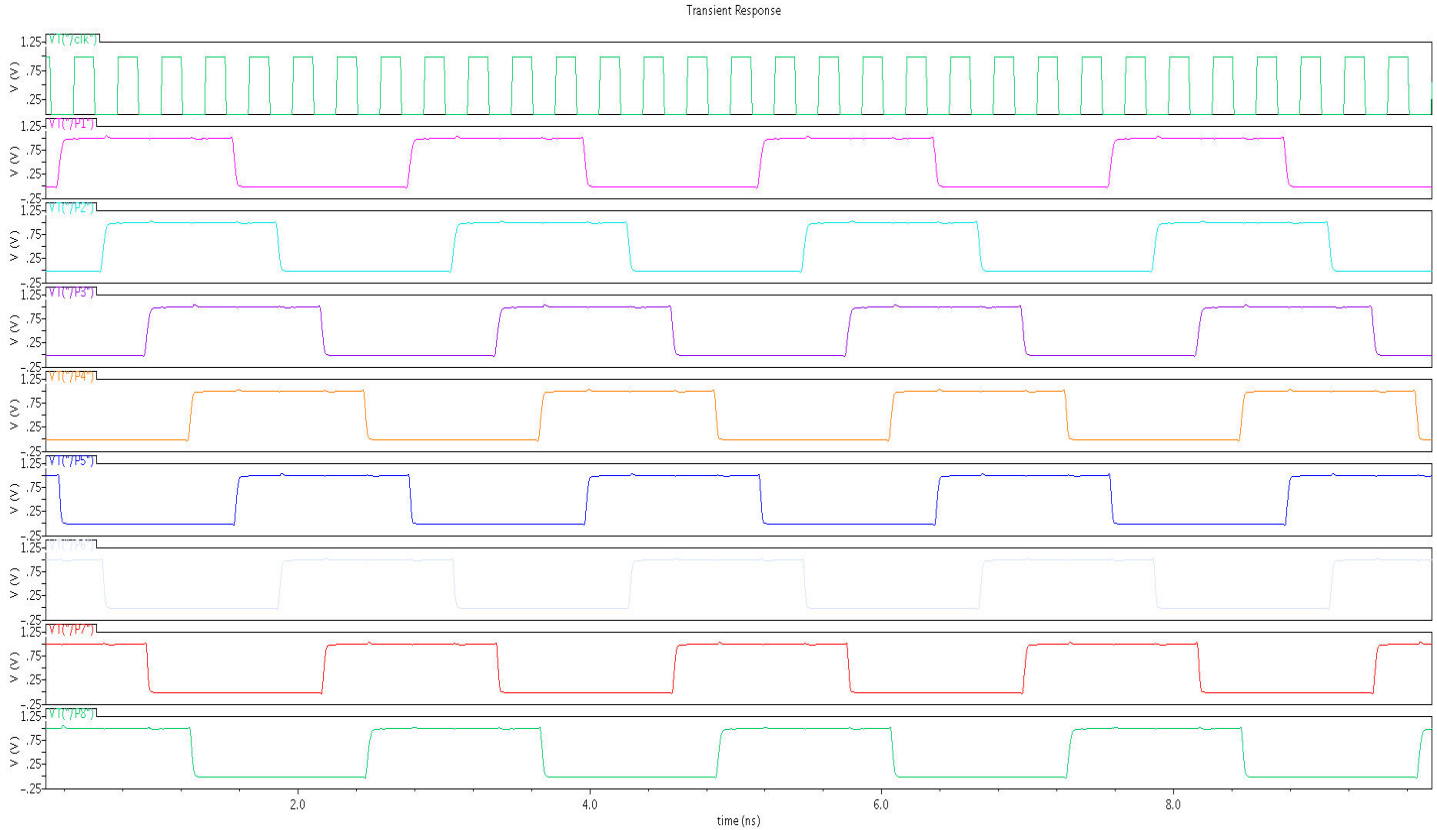
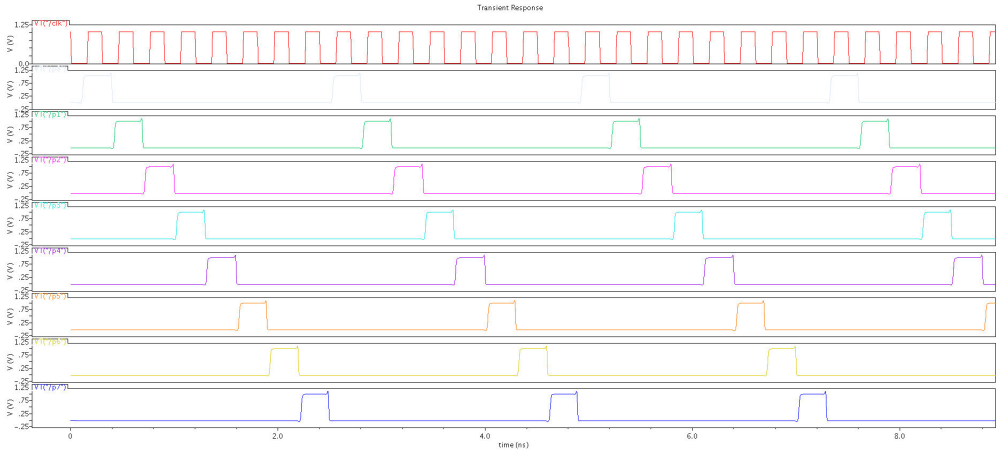
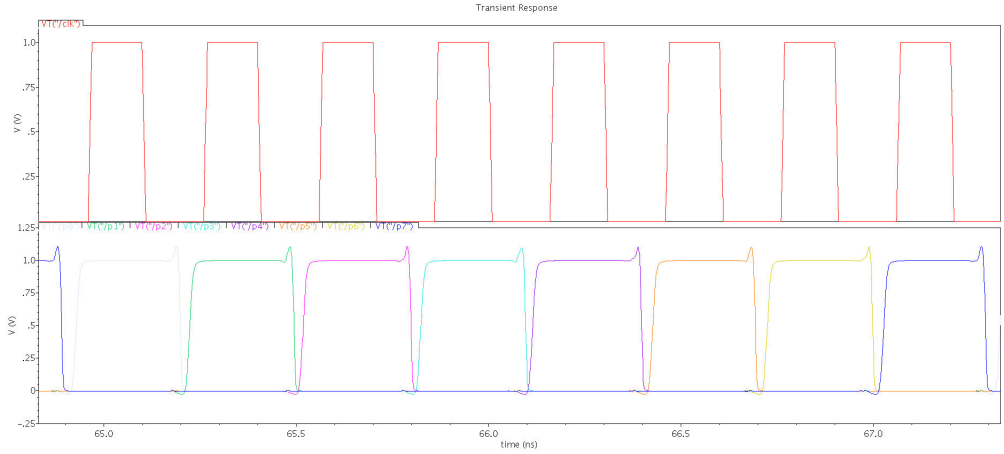


Figure 26: Eight-Phases generated by Johnson's counter



(a)



(b)

Figure 27: Modified Johnson's counter (non-OVL); (a) Output Eight-phases (b) No overlapping of phases

Two critical components in the design of a pipelined ADC are comparator and amplifier. The performance of both the components was evaluated separately. For testing the pre-amplifier based latched comparator used in this design, the circuit was supplied with a VDD of 1.2V. A bias voltage of 1V was applied to control the

current through the pre-amplifier stage. The regenerative latch circuit was clocked with time period of 0.3ns and pulse width of 0.15ns. The input signal is 1V peak-peak sinusoidal wave with a 100MHz frequency. In order to simultaneously evaluate the performance of both the input terminals same signal with inverted version of the same 1V peak-peak sinusoidal wave of 100MHz frequency was applied at the reference terminal. Output of the designed comparator is shown in Fig. 28. As evident form Fig. 28, circuit performs a fine, distortion less digital conversion of the sinusoidal input signal. The transmission delay from input to the output was observed to be 624ps. Fig. 29 shows the power consumption of the comparator circuit. The average dynamic power consumed by the whole comparator is around 1.22mW. Measured results illustrates the high performance of the designed comparator circuit.

After that, output of the fully integrated system was tested for performance evaluation. ADC was connected to an Ideal DAC block(designed in Verilog-A) and a comparison of the output with the input of the ADC was conducted, Fig. 30 shows the result of the comparison. An initial delay of around 110ns was observed, which is obvious in case of a Pipelined ADC. Performance of the circuit was further verified on different frequencies assuring Nyquist criteria, results indicate that circuit is capable of digitalizing effectively for a long range of frequencies with a small degradation in performance parameters. Fig. 31 shows the 12-bit output of the designed ADC.

Finally, the performance of the TI-ADC was verified for static and dynamic parameters. The proposed ADC design was clocked at 3.072 GHz and powered with a 1.2-V analogue supply and 1.8-V digital supply. The static performance parameters, namely the differential nonlinearity (DNL) and integral nonlinearity (INL), were tested for the individual ADCs to obtain an improved approximation,

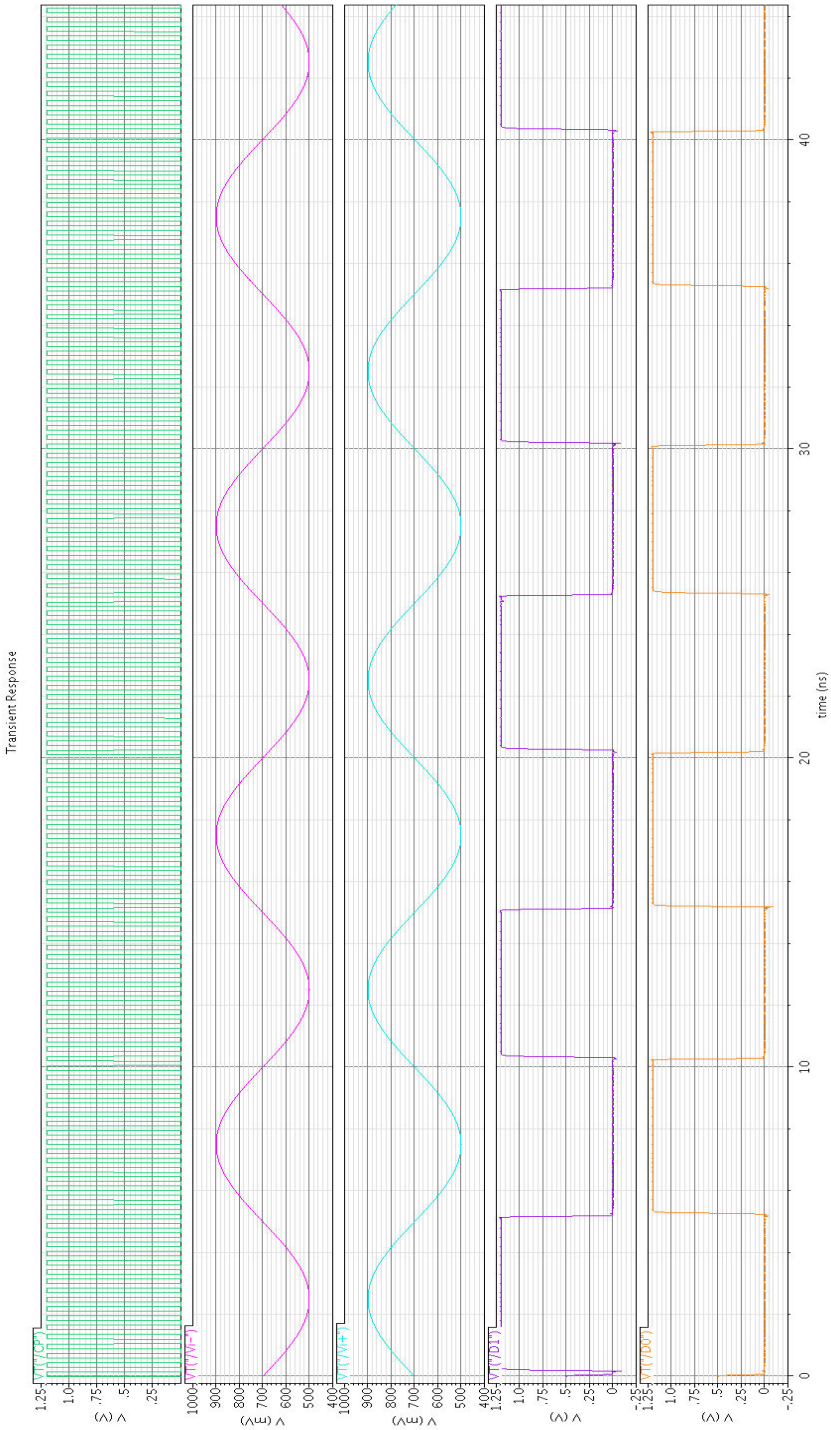


Figure 28: Simulated output of the comparator circuit

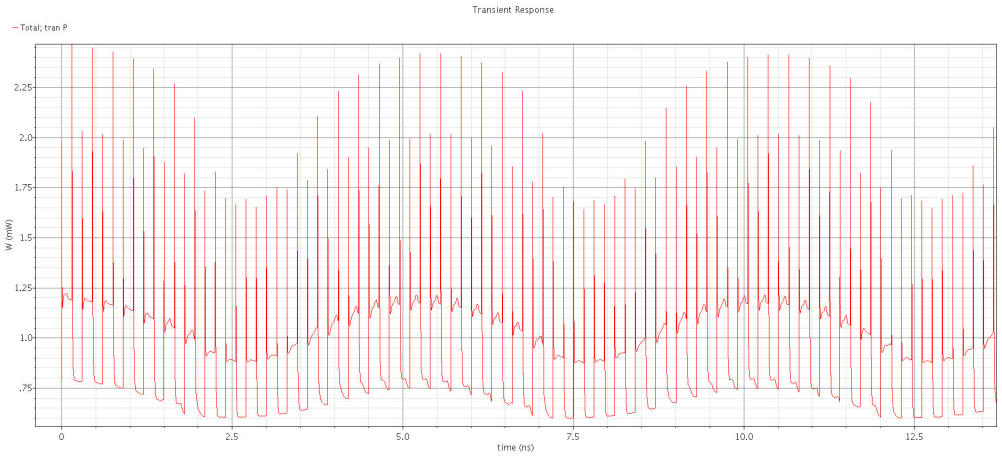


Figure 29: Power consumption of the comparator circuit

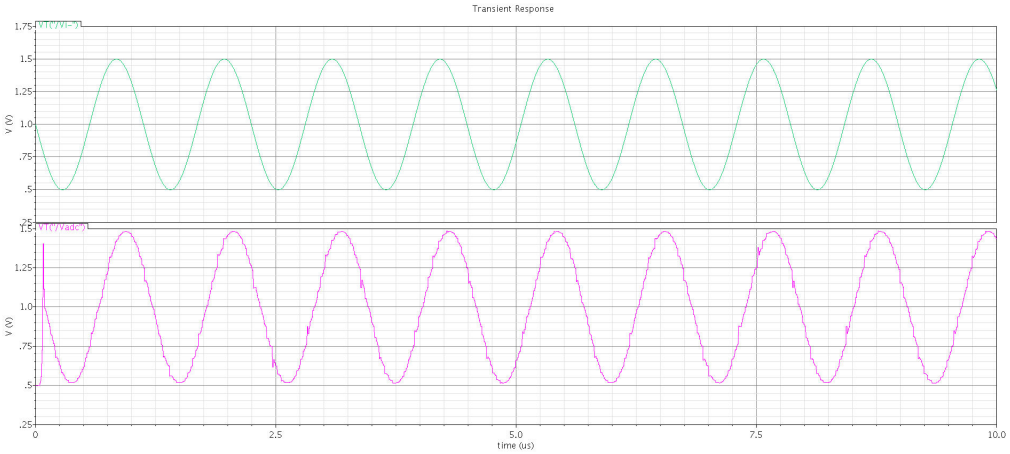


Figure 30: Comparison of input signal applied to ADC with the analog equivalent produced by the ideal DAC

while their values will be averaged elsewhere. Fig. 33b illustrates the static nonlinearity performance of the proposed design. The measured DNL values were +0.62/-0.56 LSB and the INL values were +0.57/-0.49 LSB.

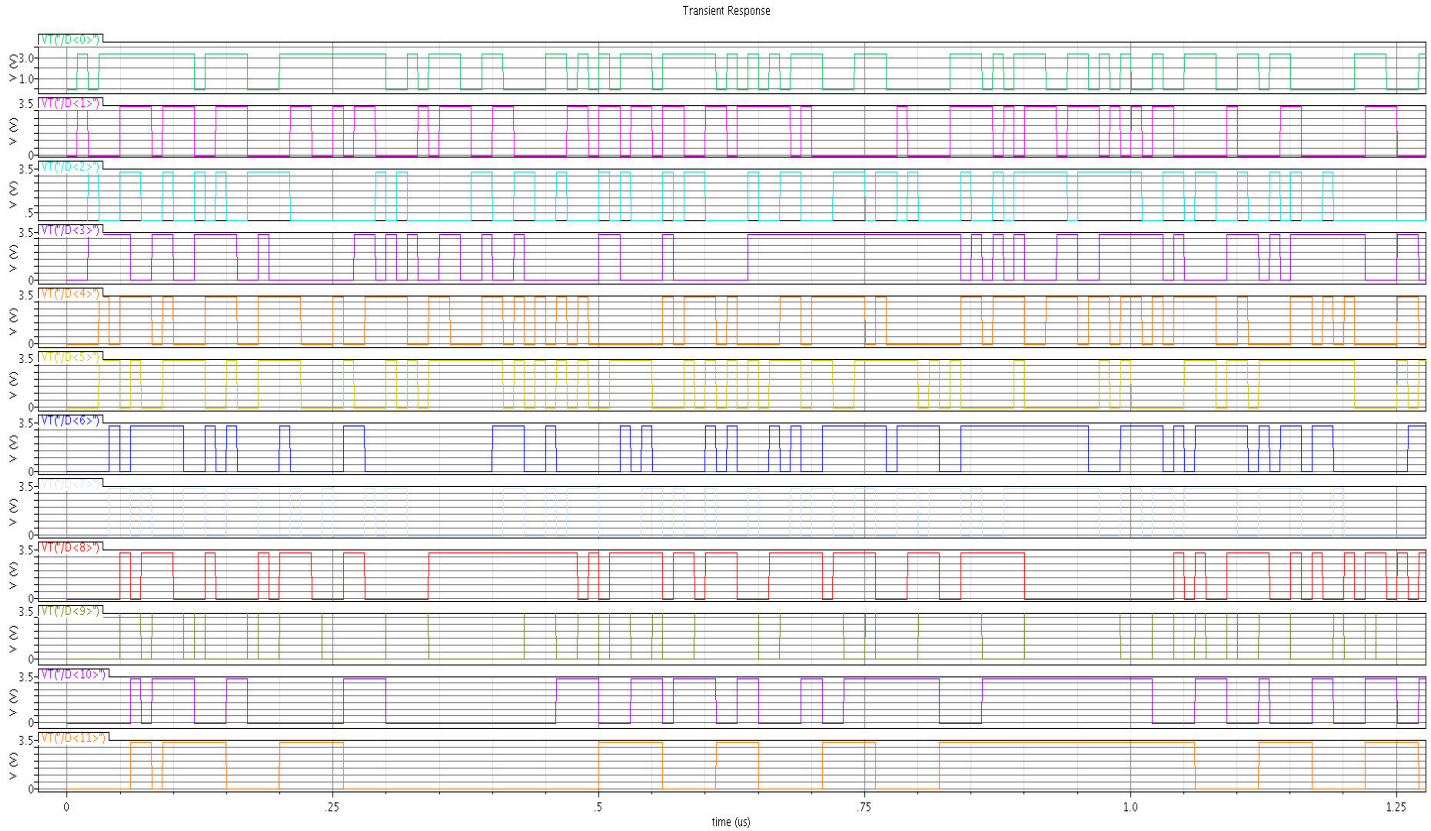


Figure 31: Digital output bits of the designed 12-bit Pipelined ADC

FInally, the performance of the TI-ADC was verified for static and dynamic parameters. The proposed ADC design was clocked at 3.072 GHz and powered with a 1.2-V analogue supply and 1.8-V digital supply. The static performance parameters, namely the differential nonlinearity (DNL) and integral nonlinearity (INL), were tested for the individual ADCs to obtain an improved approximation, while their values will be averaged elsewhere. Fig. 33 illustrates the static nonlinearity performance of the proposed design. The measured DNL values were +0.62/-0.56 LSB and the INL values were +0.57/-0.49 LSB.

For the dynamic performance, the output spectrum of the proposed TI-ADC after digital background calibration at an input frequency of 467 MHz is illustrated in Fig. 32. The measured SNDR and SFDR values were 53.65 and 69.04 dB, respectively. The performance limitation owing to the elevated noise floor in the output spectrum is mainly attributed to the comparator circuit, which is the result of the selected trade-off for increasing the comparator speed. In order to validate the performance of the proposed design for its use in wideband fully digital receiver applications further, the design was swept across a wide range input frequency between 40 kHz and 1 GHz. The variations in the SFDR and SNDR values at different input frequencies are presented in Fig. 34. The designed circuit inhabits an effective resolution bandwidth of more than 890 MHz in a 1 GHz band. The SFDR values are approximately 70 dB and are maintained across the entire band, which further demonstrates the effectiveness of the proposed design for this application.

Fig. 35 and Fig. 36 present a comparison of the figure-of-merit (FoM) of this design with other available state-of-the-art designs (with respect to the conversion rate and effective resolution bandwidth (ERBW)). The proposed design consumes 820 mW of power operating at a 1.2-V supply, which, according

to Walden's FoMs, which evaluates to 0.67 pJ/conv.-step. As is evident from the above figures, the proposed designed outperforms other state-of-the-art high-sampling ADC designs in terms of speed, bandwidth, and efficiency. A detailed comparison with state-of-the-art high-speed designs is presented in Table 1.

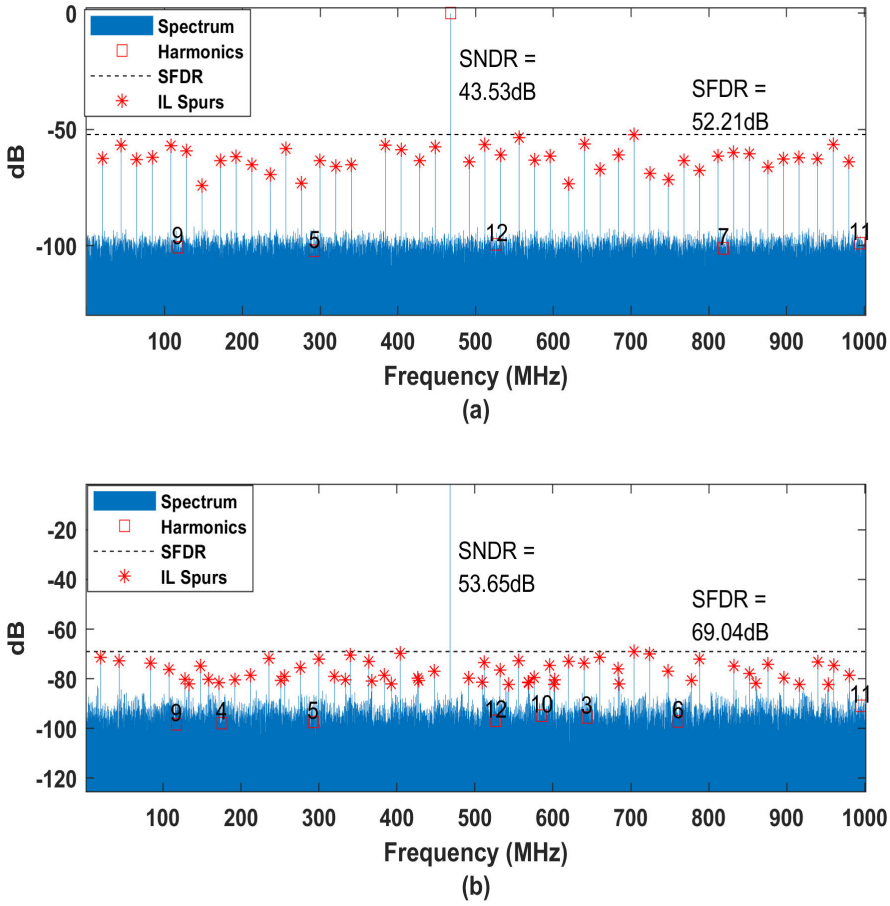
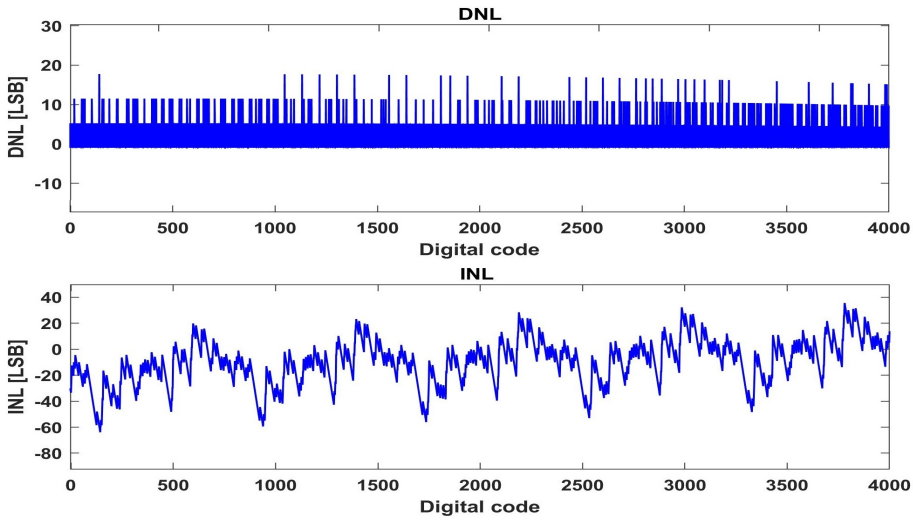
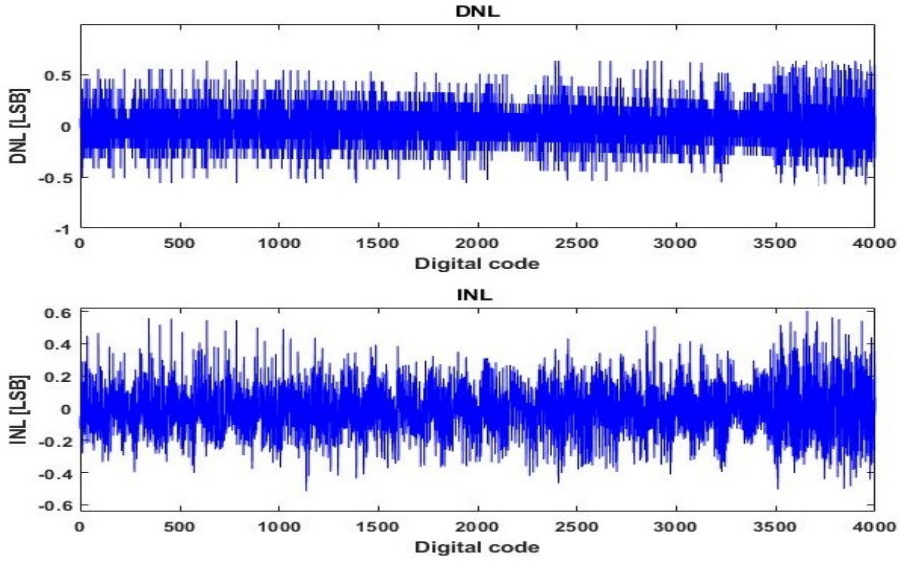


Figure 32: Measured output spectra at 467 MHz input



(a)



(b)

Figure 33: (a) Before Calibration Measured DNL and INL. (b) After Calibration Measured DNL and INL.

Table 1: Performance Summary and Comparison

Parameters	**[23] Flash ADC**	**[24] MDAC Eq.**	**[25] TI-SAR ADC**	**This Work**
Technology	130nm	40nm	65nm	65nm
Resolution	5b	12b	10b	12b
$F_s[Hz]$	3.2G	2.1G	1G	3.072G
SNDR [dB]	29.09	52	51.04	53.65
ENOB	4.54	8.34	8.19	8.61
ERBW [Hz]	600M	600M	500M	890M
FoM [pJ/conv.]	4.3	0.43	0.0623	0.67

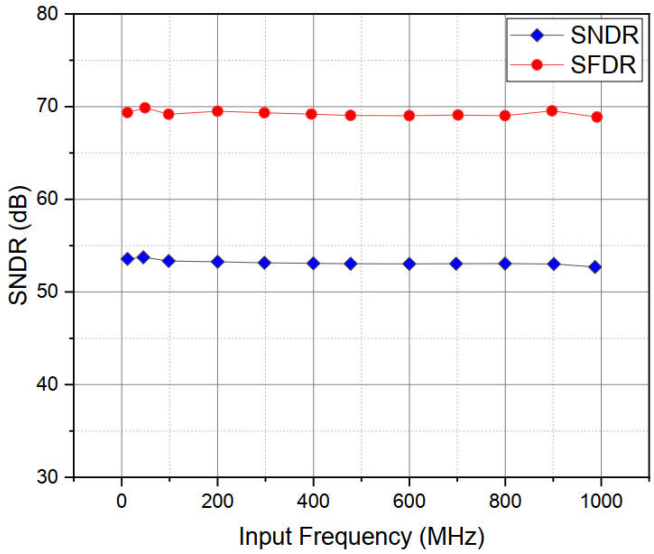


Figure 34: Measured SNDR and SFDR at 3.072 GS/s

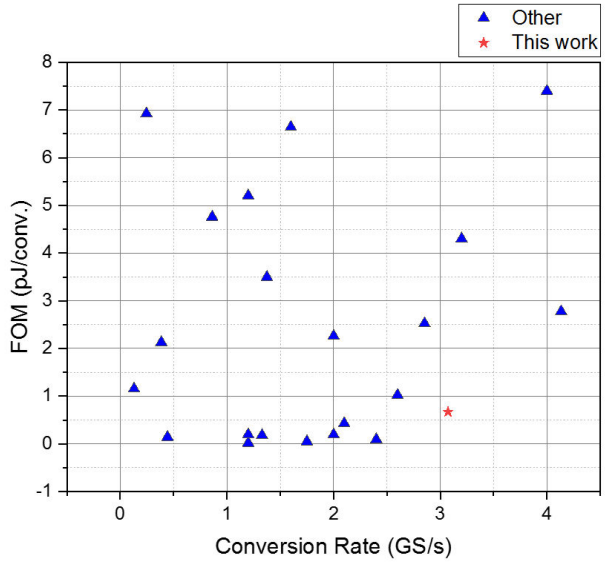


Figure 35: Comparison of figure-of-merit w.r.t. conversion

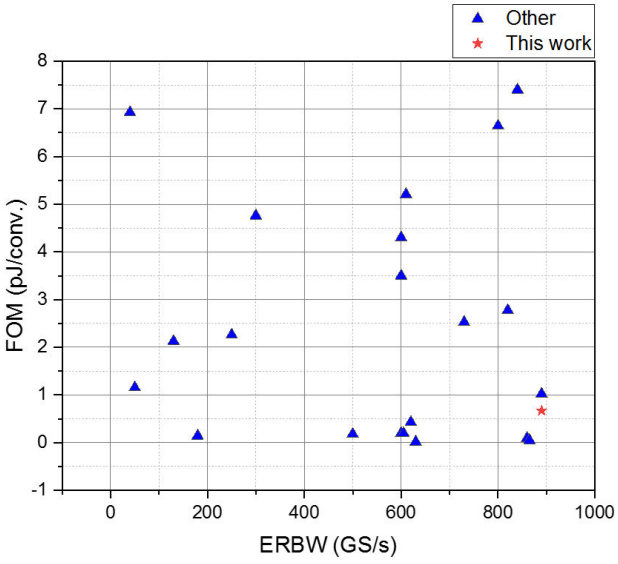


Figure 36: Comparison of figure-of-merit w.r.t. ERBW

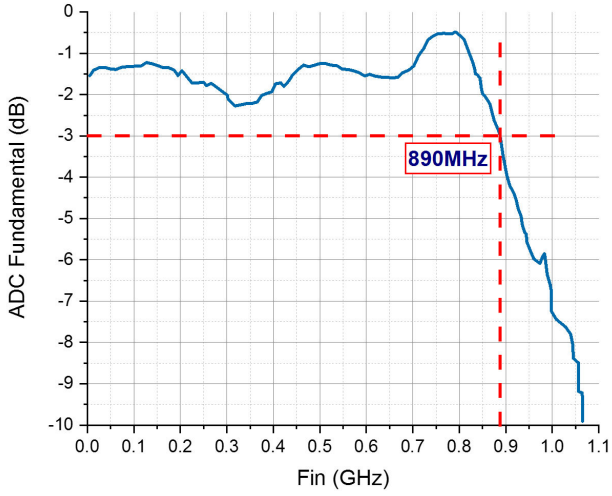


Figure 37: Bandwidth of the TI-ADC

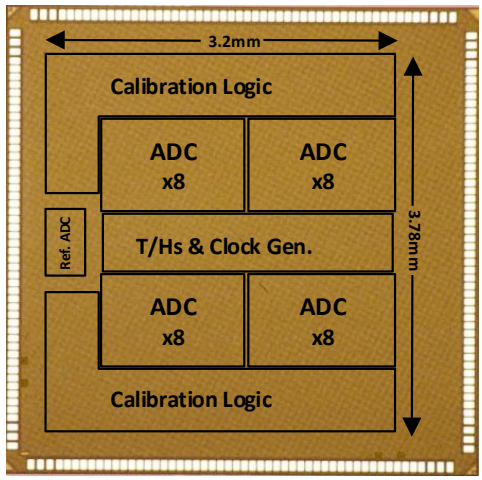


Figure 38: Chip micrograph Samsung 65nm CMOS

IX. CONCLUSION

In this work, a 12-bit 3.072GS/s ADC was designed, in which 32 pipelined ADCs were interleaved, each with an individual sampling rate of 96 MS/s.

- The proposed design provides power efficiency, which was made possible by adopting the amplifier-sharing technique in the *S&H* structure of the TI-ADC and using an equal number of bits for all stages of the sub-ADC.
- The use of high-performance components, such as the pre-amplifier latch-based comparator and gain-boosting amplifier, assures the speed efficiency of the design, while satisfying the high bandwidth and linearity requirements of the system.
- The implemented digital background calibration scheme is simple, and effectively mitigates the effects of gain, offset, and timing skew mismatches.

As a result, the proposed technique provides a higher sampling speed and ERBW compared to other state-of-the-art designs, making it a perfect candidate for use in wideband applications.

PUBLICATIONS

A. Journals

1. W. H. Siddiqui and G. S. Choi, "Time-Interleaved Pipelined Analog to Digital Converter for Wideband Full Digital Re-ceiver" *Submitted for review in IET Circuit, Devices and systems*.

B. Conferences

1. W. H. Siddiqui and G. S. Choi, et al."Low-power High-speed comparator for TI-ADC in 65nm CMOS Technology," in *IEIE FALL CONFERENCE*, 2018.

2. S. K. Mostaque, W. H. Siddiqui, A. Ferdousi, G. S. Choi, et al."A Development of an Inner Tube Inspection and Cleaning Robot System," in *Korean Society of Electronics Engineering Autumn Conference*, 2017.

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