[UCI]I804:24011-200000266761

2018年 2月

博士學位 論文

직병렬 구조를 갖는 스위치드 커패시터 멀티레벨 인버터에 관한 연구

朝鮮大學校 大學院

電 氣 工 學 科

尹 京 錫

직병렬 구조를 갖는 스위치드 커패시터 멀티레벨 인버터에 관한 연구

A Study on the Switched-Capacitor Multi-Level Inverter with Series/Parallel Structure

2018年　2月 23日

朝鮮大學校 大學院

電氣工學科

尹　京　錫

직병렬 구조를 갖는 스위치드 커패시터 멀티레벨 인버터에 관한 연구

指導敎授 曺 錦 培

이 論文을 工學博士學位 申請論文으로 提出함

2017年 10月

朝鮮大學校 大學院

電氣工學科

尹 京 錫

尹京錫의 博士學位論文을 認准함

委員長 朝鮮大學校 敎授 崔孝祥 印

委 員 朝鮮大學校 敎授 金南默 印

委 員 한국폴리텍대학 敎授 金賢哲 印

委 員 朝鮮大學校 敎授 崔然玉 印

委 員 朝鮮大學校 敎授 曺錦洽 印

2017年 12月

朝鮮大學校 大學院

Contents

List of Tables

List of Figures

ABSTRACT

직병렬 구조를 갖는 스위치드 커패시터 멀티레벨 인터버에 관한 연구

Kyoung Seok Yoon
Advisor : Prof. Cho Geum Bae, Ph.D.
Department of Electrical Engineering
Graduate School of Chosun University

최근에 스위칭 소자를 많이 사용하는 전력전자분야에서 전력용 스위칭 소자의 전압 스트레스 감소, 전압변동률의 저감, EMI의 감소로 멀티 레벨 인버터에 관한 연구는 기업체나 연구자의 주요 연구 테마 중 하나이다. 멀티 레벨 인버터 분야에 관한 대표적인 토폴로지는 NPC(Neural Point Clamped), FC(Flying Capacitor), 캐스케이드 H-브리지(Cascaded H-Bridge) 방식의 인버터가 있으며 지속적인 연구개발을 통하여 다양한 토폴로지가 제안되고 있다. 하지만 기존의 멀티 레벨 인버터 구성은 많은 스위칭 소자, 다이오드, 커패시터, 인덕터 등을 사용하기 때문에 인버터 비용의 상승과 제어가 복잡해지는 단점을 가지고 있다. 따라서 본 논문에서는 직병렬 구조를 갖는 스위치드 커패시터 멀티 레벨 인버터 (Switched Capacitor Multilevel Inverter, SCMI)의 새로운 토폴로지를 제안하였다. 기존의 멀티 레벨 인버터와 마찬가지로 제안 된 SCMI의 기능은 동일하지만 적은 스위칭 소자와 부품을 사용함으로써 시스템의 사이즈를 줄여 가격 경쟁력의 향상, 인버터의 성능 및 신뢰성을 향상시킬 수 있다. 또한 제안 된 토폴로지에서는 커패시터를 사용함으로써 출력 전압은 변압기를 사용하지 않고 승압이 가능하고 보조 회로를 사용하지 않고 전압 밸런싱 문제를 해결 할 수 있도록 구성하였다. 이러한 제안된 직병렬 구조를 갖는 스위치드 커패시터 멀티레벨 인버터 방식에 관한 이론적 고찰을 통한 분석과 PSIM을 이용한 시뮬레이션 수행과 실험을 통해 입증하고 그 타당성을 검증하고자 하였다.

Ⅰ. Introduction

A. Background

Nowadays, with developing of science, fuel cells are being developed to replace the traditional batteries and accumulators. Fuel cell transforms the chemical energy of fuels, such as hydrogen, directly into electrical energy. Fuel cells are energy devices, which almost doesn't populate, so it contributes to global climate development in the long term and bring more benefits to the ecosystem.

The fuel cells are used to storage and provide electricity. However, the power is generated from the fuel cells are a direct current source, to be able to use this power supply for AC devices such as motors, machinery, equipment, this power should be converted into alternating current source. A component has an important role in converting DC power to AC power is inverters.

During a few years, power electronics is the new researching and has developed significantly, which has two major topics. The first, this is the development of semiconductor devices that are high speed, high voltage capability and high power applications. The second topic is focused real-time controllers that can develop complex and advanced control strategies. With the development of power electronics devices, digital controllers, and sensors, the power inverters are commonly used in many applications such as AC motor drives, uninterruptible power supplies (UPSs), hybrid electric vehicles and distributed power systems. The major function of the power inverter is to produce an output AC voltage from an input dc voltage. There are many different ways to control the output AC voltage of an power inverter. The most method consists of controlling the PWM applied to the power semiconductor devices such as IGBTs, MOSFETs, GaNs, etc. Based on the

waveform of the output voltage, power inverters have three types as: square wave inverters, two-level PWM inverters, and multi level inverters. The traditional two-level PWM inverters have following problems. Firstly, the peak AC output voltage is lower than the DC source voltage, in the other hand, the traditional two-level PWM inverters can only provide buck dc-ac power conversion. So, they are unsuitable for the interface between renewable energy sources (such as wind, photovoltaic and fuel cells) and grid where a low dc input source voltage is inverted to a high output voltage. The secondly, the voltage stress across switching devices and electromagnetic interference (EMI) are very high. So, the efficiency is low because the switching loss of semiconductor is high. The thirdly, A high common-mode voltage is produced and thus, when two-level PWM inverters are used to control motor, the stress in the bearings is very high. Besides that, THD of output voltage are very high. To alleviate the aforementioned drawbacks of the traditional two-level PWM inverters, the multi level inverter structure has been proposed as an alternative in medium voltage and high power applications. multi level inverter used power switches along with many low-voltage dc levels to provide the power conversion. Batteries, and renewable energy voltage sources and capacitors was used as the input dc levels. The multi level inverters are becoming wide interest both in the industry and in the research community from the time when the multi level inverter was introduced. A stepped output voltage are produced by arranging power semiconductor switches and required dc voltage sources. The number of levels decides the number of input dc voltages. And, when the levels of output voltage are rised, THD are reduced. PWM method is the major method implemented in power conversion and the effective way of driving power semiconductor switches. PWM signals of various forms with multiple carrier arrangements of two types: phase shifted and level shifted were used to control most of the power conversion.

The major advantages for the multi level inverters are presented as following.

- They are appropriate in high output voltage and power levels application.
- They are suitable for the interface between renewable energy sources and grid.
- The efficiency is higher because the switching loss of semiconductor is reduced.
- By using some control strategies of multi level inverter, the high power quality and stability of the system can be achieved.
- The voltage stress across switching devices and electromagnetic interference (EMI) are eliminated.
- Because of the modular structure, the levels of the output voltage can be increase to unlimited levels.

Multi level inverters have many different topologies. However, Cascade H-bridge, Flying capacitor and Neutral point clamped are three basic topologies. Although three basic topologies are used in high power applications, three basic topologies have many demerits. The major demerit of Neutral point clamped topology is unbalanced voltage. Moreover, The Neutral point clamped topology is required for higher number of clamping diodes. In Flying capacitor topology, flying capacitor are used as clamping device. However an excessive number of storage capacitors is required for high-voltage application. Among these topologies, Cascaded H-bridge is an effective topology for high-voltage application due to simplicity of control and its modularity. The power and voltage level can be scaled easily because the cascaded H-bridge topology consist of many power conversion modules connected in series together. However, because each H-bridge cell in the cascaded H-bridge topology is required a separate dc source. So, the cascaded H-bridge topology becomes complex and expensive to implement.

To address the aforementioned drawbacks, the other topologies with using of a single dc source were proposed. So, this structure limited the cost. And, it is called hybrid cascaded H-bridge topology. Furthermore, the number of required switches is reduced. So, it can improve EMC and reliability.

This paper presents a new SCMI configuration which combines with the H-bridge circuit to create output ladder voltage waveform in reducing the number of switches. The proposed SCMI does not use any inductors. This paper develops the theoretical operation of the proposed SCMI and verifies the operating principle through the simulation result of nine-level configuration by PSIM 9.0 software. The proposed SCMI is extended to n-level by adding the SC cells. The study results are also demonstrated through experiments with inverter 9-level.

B. Scope of the Dissertation and Organizations

The objective of this dissertation is investigated on the development of multi level inverter structures. And then, proposing a novel multi level inverter structure to reduce the number of semiconductor switches, input sources, thereby reducing the cost and size of the system compared to the previous configurations.

The dissertation is organized as follows:

In Chapter 1 is an introduction to some of the previous research in multi level inverter based on a review of current literature.

A discussion of multi-level inverter topology and the modulation techniques based multi-carrier PWM methods is provided in Chapter 2. Several power converter candidates are discussed and compared, including: used as the neutral-point-clamped (NPC, the flying capacitor (FC) and the cascade H-bridge (CHB)

In Chapter 3 a new switched-capacitor multi level inverter (SCMI) topology has been proposed

In Chapter 4 an extended circuit topology of proposed SCMI for $(2^{n+1}+1)$ level is illustrated.

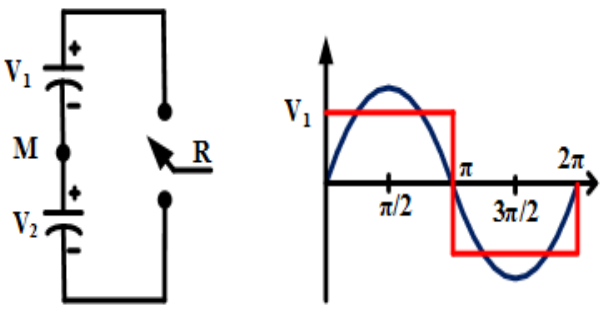
In Chapter 5 shows the simulation and experimental results of the system.

In Chapter 6 summarizes the research work included in this dissertation and gives future research directions.

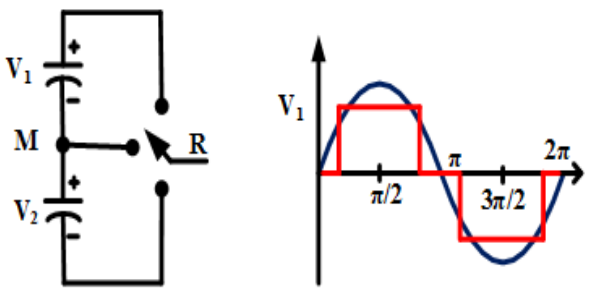
Ⅱ. Multi Level Inverter Topology Surveys

Recently multi-level inverter technology have become more attractive for researchers and manufacturers because they have some advantages over the conventional three-level pulse width modulation (PWM) inverters. The multi level inverter has the following advantages as improved output waveform quality, lower electromagnetic interference (EMI) and lower device stress [1]-[4]. Multi-level inverters include semiconductor switches capacitors, diodes, and supplies. When the switches are switching to supply the capacitor voltages, which increases the step-up gain ratio of the output voltage, while the voltage stress on the power semiconductors are reduced significantly. The multi-level inverter configuration is commonly used as neutral point clamped (NPC); capacitor-clamped (flying capacitors); and cascaded H-bridge inverter with separate dc sources. The most attractive features of multi-level inverters are that they improved output waveforms with lower THD, and they can operate with a lower switching frequency and smaller filter size and lower EMI.

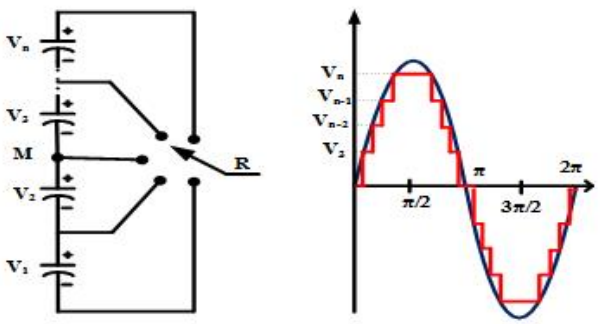
As shown in Fig. 2-1, the synthesized output can be achieved by dividing the dc-link voltage into multiple sections. So the each phase leg can be switched and has multiple voltage levels. For example, as shown in Fig. 2-1(a), a two-level inverter generates two output voltage levels. From Fig. 2-1(b), the three-level can produce three while the generalized n-level inverter is able to switch among n-level voltage as shown in Fig. 2-1(c) Neutral-Point-Clamped (NPC) inverter topology [5]-[7], is introduced by Nabae in 1980s. NPC inverter provides the clamping voltage across the switches by diodes and capacitors. As result, the diodes should be connected as series, which causes the problem of the design, reliability system and cost.



(a) Two-level



(b) Three-level



(c) N-level converter

Fig. 2-1 Simplified circuit

Flying Capacitor (FC) Inverter [8] - [9] was proposed by Meynard and Roch in 1992 to replace the clamping diodes by flying capacitors. By using extra states where the same output voltage level can be achieved when the switching is combined together, FC inverter can create a freedom state to balance the flying capacitor. However, similar to the blocking requirements of the clamping diodes, the flying capacitors are submitted to different voltage levels. A large number of bulk capacitors are required in the FC inverter to clamp the voltage. So as to eliminate extra clamping elements (capacitors and diodes) and to eliminate voltage unbalance, the Cascaded Full-Bridge Inverter [10] - [15] has been proposed. The Cascaded Full-Bridge Inverter is suitable for medium and high power applications due to its advantages in modularization and extensibility. The basic idea of single phase full-bridge inverters connected in series with multiple isolated dc supplies to realize multi level waveforms. This researching has been extended for three-phase applications, such as drive applications, etc. These configurations use a large number of components including semiconductor switches, power supplies, capacitors and diodes. As a result, the overall system has a high cost and complex control.

A. Classification of multi level inverter

1. Neutral-point clamped multi level inverter

Assume that the DC power supply is divided into several smaller voltages due to series capacitors. Each leg of a three-phase n-level NPC converter is devised of 2*(n-1) connected to switches in series and (n-1) capacitors in series charged with a voltage of $V_{dc}/(n-1)$. By using balanced voltage condition, the stress voltage on the switches is the each voltage capacitor.

Fig. 2-2 illustrates one leg of a three-level diode clamped multi-level structure. In this circuit, the DC input voltage is split into three levels by two series-connected capacitors, C_1 and C_2. The output voltage is VAN where N is chosen as the neutral point. The output voltage V_{AN} has three states:

· VAN =Vdc/2 : switches S1 and S2 need to be turned on
· VAN =0 : switches S1 and S3 or switches S2 and S4 need to be turned on.
· VAN =-Vdc/2 : switches S3 and S4 need to be turned on

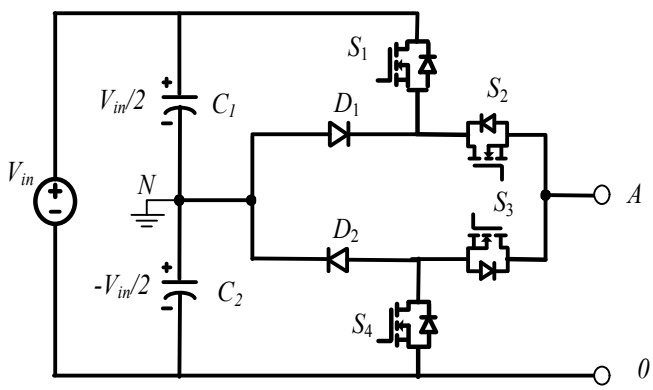


Fig. 2-2 Three-level neutral-point clamped inverter topology

Fig. 2-3 shows the five-level NPC inverter is shown in. The DC input voltage is divided into four capacitors C_1, C_2, C_3 and C_4, that allows the output voltage of inverter with five levels voltage and limits by the blocking voltage switch to $V_{dc}/4$. The output voltage V_{AN} and the corresponding switch state are shown in Table 2.1

Table 2-1 Switching states for a five-level neutral-point clamped inverter

Output V_{an}	Switch state							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{an}=\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$V_{an}=\frac{V_{dc}}{4}$	0	1	1	1	1	0	0	0
$V_{an}=0$	0	0	1	1	1	1	0	0
$V_{an}=-\frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$V_{an}=-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

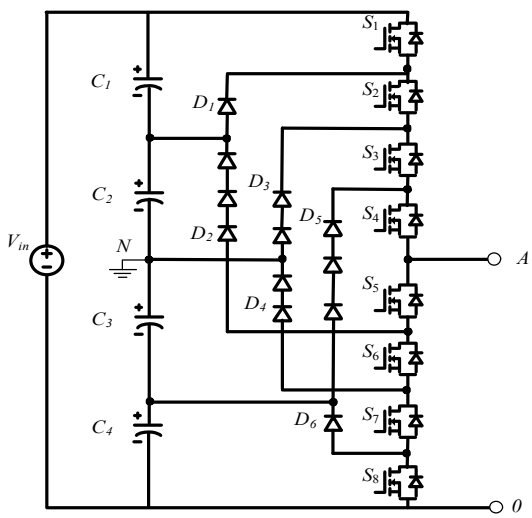


Fig. 2-3 Five-level neutral-point clamped inverter topology

2. Capacitor-clamped multi level inverter

The topologies of the three-level and five-level capacitor-clamped (NPC) multi level inverter are illustrated in Fig. 2-4. The topology is similar structure as the diode-clamped multi level inverter. However, diodes was replaced by the capacitors.

The output voltage V_{AN} has three states:

· $V_{AN} = V_{dc}/2$: switches S_1 and S_2 need to be turned on

· $V_{AN} = 0$: switches S_1 and S_3 or switches S_2 and S_4 need to be turned on.

· $V_{AN} = -V_{dc}/2$: switches S_3 and S_4 need to be turned on

Fig. 2-5 shows a five-level capacitor-clamped converter topology. The voltage synthesis in a five-level NPC inverter has more flexibility than a NPC inverter. Table 2.2 shows the switch state of a level-five capacitor-clamped inverter.

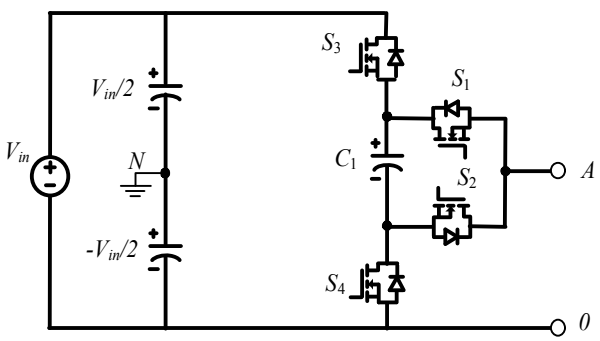


Fig. 2-4 Three-level capacitor -clamped inverter topology

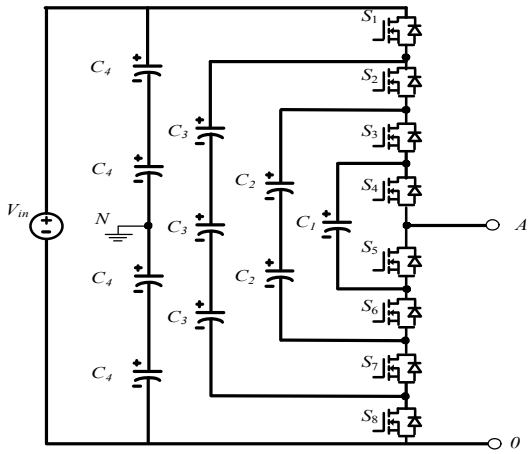


Fig. 2-5 Five-level capacitor-clamped inverter topology

Table 2-2 Switching states for a 5 level capacitor-clamped inverter

Output V_{an}	Switch State								Capacitor combination
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
$V_{an}=\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0	C_4
$V_{an}=\frac{V_{dc}}{4}$	1	1	1	0	1	0	0	0	$C_4 - C_1$
	1	0	1	1	0	0	1	0	$C_4 - C_3 + C_2$
	0	1	1	1	0	0	0	1	$C_3 - C_4$
$V_{an}=0$	1	1	0	0	1	1	0	0	$C_4 - C_2$
	0	0	1	1	0	0	1	1	$C_2 - C_4$
	1	0	1	0	1	0	1	0	$C_4 - C_3 + C_2 - C_1$
	0	1	0	1	0	1	0	1	$C_3 - C_2 + C_1 - C_4$
	0	1	1	0	1	0	0	1	$C_3 - C_1 - C_4$
$V_{an}=-\frac{V_{dc}}{4}$	1	0	0	0	1	1	1	1	$C_4 - C_3$
	0	0	0	1	0	1	1	1	$C_1 - C_4$
	0	0	1	0	1	0	1	1	$C_2 - C_1 - C_4$
$V_{an}=-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1	$-C_4$

3. Cascaded multi level inverters

Fig. 2-6 shows the cascaded multi level inverter topology. It based on the series connection of full-bridge inverters with directly connect with DC sources. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. The output voltage of each single-phase full-bridge inverter is 3-level: $+V_{dc}$, 0, $-V_{dc}$.

- To generate a positive $+V_{dc}$: two switches S_1 and S_4 have been turned on.
- Output voltage equal to $-V_{dc}$: two switches S_2 and S_3 have been turned on
- To produce a zero voltage: either S_1 and S_2 or S_3 and S_4 have been turned on

This topology is suitable for medium and high power applications with some advantages in modularization and extensibility. Compared to previous topologies, to achieve the same number of levels the required number of components is reducing.

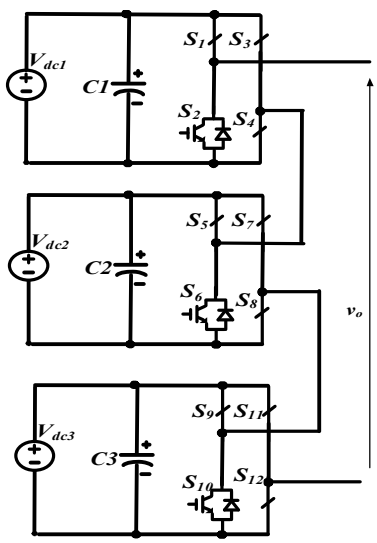


Fig. 2-6 Cascaded multi-cell multi level inverter circuit topology

4. Conventional switch capacitor multi level inverters

Fig. 2-7 shows the SC nine-level inverter with a single dc source. It was presented in [54] with using a large number of switch. Fig. 2-8 shows a combination of Switch capacitor cells for Switch capacitor multi level inverters [55]-[56]. Each SC cell contains one diode, one capacitor and two switches. These topologies can boost voltage without the inductor. Moreover, the capacitor voltage in these topologies can be self-balance. The amount of the components in the circuit is lower than that in the traditional multi level inverters, it is still high though.

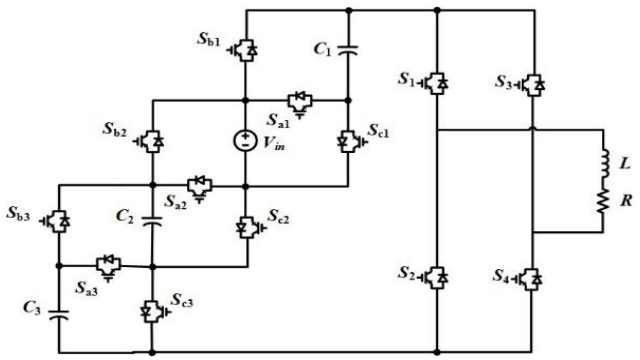


Fig. 2-7 Conventional SC-based nine-level inverters topology with series/parallel conversion [18]

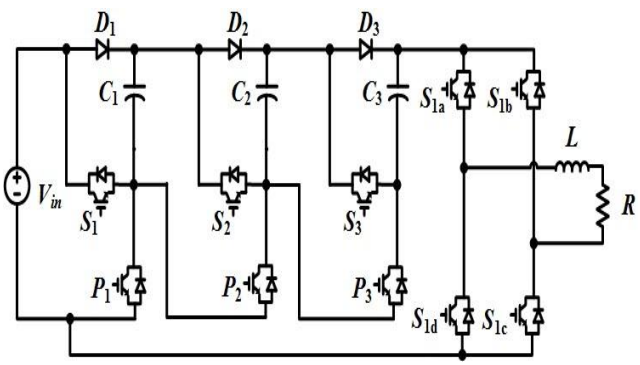


Fig. 2-8 Hybrid topology using SC units [20]

B. Modulation and Control Strategies

Most carrier-based PWM schemes for diode-clamped and capacitor-clamped inverter derive from the carrier disposition strategy were discussed in the past research. In the N-level inverter topology, the strategy disposes N-1 triangular carriers with similarly the frequency and amplitude. Thus, they take the bands over the range $+V_{dc}$ to $-V_{dc}$. The single sinusoidal reference is used to compare with each N-1 triangular carriers to generate the output voltages for the inverter. The rotational carrier PWM strategies are used as following.

1. Multi Level Selective Harmonics Elimination Technique

The selective harmonics elimination technique or fundamental switching frequency technique is well-known method that used to eliminate the lower order harmonics from the output voltage waveform of the multi level inverter [68]. In selective harmonics elimination technique, the intersection of the triangular carrier and the modulation waveform calculates the generation of the pulse. Consequently, the carrier frequency is much higher than the modulation frequency. The generated rectilinear output voltage pulses are modulated such that their duration is proportional to the instantaneous value of the sinusoidal waveform at the center of the pulse. The pulse area is proportional to the corresponding value of the modulating sine wave. If the carrier frequency is very high, an averaging effect occurs, resulting in a sinusoidal fundamental output with high-frequency harmonics, but minimal low-frequency harmonics. For solving the complex equations in the selective harmonics elimination technique, many optimization algorithm techniques can be applied.

2. Phase Disposition(PD) and Phase Opposition Disposition(POD) Techniques

The PD-PWM method optimizes the harmonic voltages of a multi level inverter. The method adjusts the position and amplitude of the carrier signals to find the optimum values. This minimizes the total harmonic distortion of the output voltages. Fig. 2-9 shows the PD-PWM method where all carriers in phase. Another approach is phase opposition disposition (POD), where the carriers above the sinusoidal reference zero point are 180° out of phase with those below the zero point as shown in Fig. 2-10.

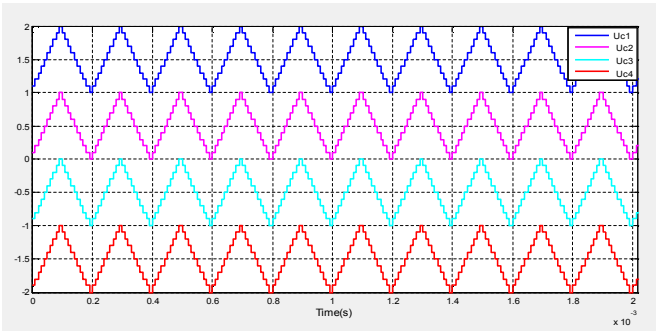


Fig. 2-9 Control technique with Phase Disposition

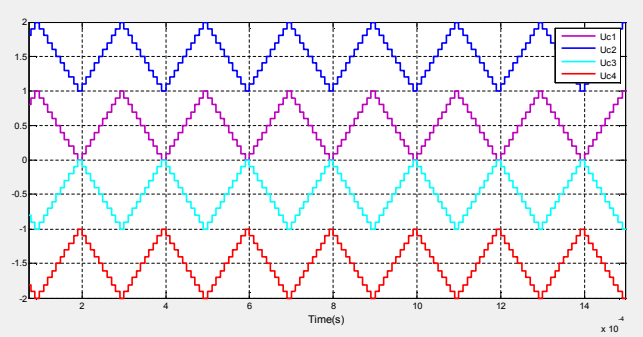


Fig. 2-10 Control technique with Phase Opposition Disposition

3. Alternative Phase Opposition Disposition(APOD) Techniques

In the alternative phase opposition disposition (APOD), each carrier is phase shifted by 180° from its adjacent carrier as shown in Fig. 2-11. For the cascaded inverter, phase-shifted carrier PWM as shown in Fig. 2-12 is the most common strategy, with an improved harmonic performance of the output voltage can be achieved when each single-phase inverter is controlled using three-level modulation.

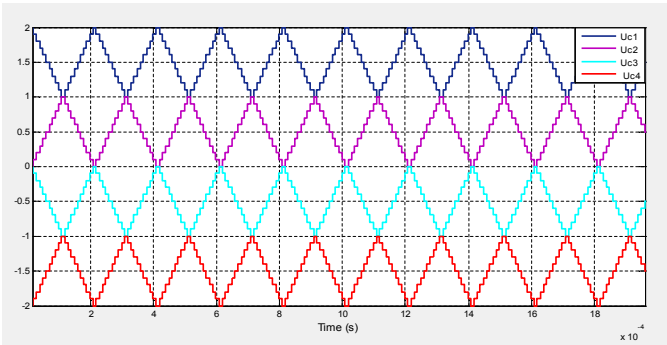


Fig. 2-11 Control technique with Alternative Phase Opposition Disposition

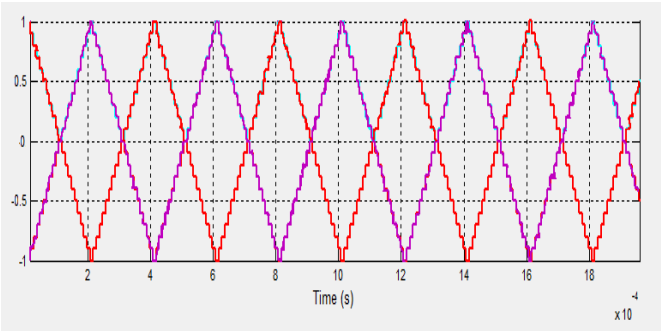


Fig. 2-12 Control technique with Phase-Shifted PWM

Ⅲ. Proposed SC Nine-Level Inverter

A. Introduction

The multi level inverter (MI) is one of the important components in the power electronics field. However, the conventional configurations MIs use a large number of components including semiconductor switches, power supplies, capacitors, inductors and diodes. As a result, the overall system has a high cost and complex control.

In order to solve the problems in the traditional MIs, a switched-capacitor (SC) structure is added to the MI to boost voltage [16]-[26]. The switched-capacitor multi level inverter (SCMI) uses charging and discharging characteristics of the capacitor to reduce the number of the source in the circuit. The SCMI can be self-balance by switching the capacitors in parallel and in series through the switches. In the parallel mode, the capacitors are charged directly by power supply, while they release store energy during the series mode. By using SC structures, the system does not need more power supplies to increase the output voltage level or the transformers to boost output voltage. In the SCMI, the H-bridge circuit is generally used to change the state of the output voltage.

This paper presents a novel SCMI configuration which is combined with the H-bridge circuit to create output ladder voltage waveform in reducing the number of switches. The proposed SCMI does not use any inductors. This paper develops the theoretical operation of the proposed SCMI and verifies the operating principle through the simulation result of nine-level configuration by P.SIM 9.0 software. The proposed SCMI is extended to n-level by adding the SC cells. The study results are also demonstrated through experiments with inverter 9-level.

B. Proposed Topology

Fig. 3-1 shows a proposed SC nine-level inverter topology. The proposed SCMI consists of two SC cells connected in parallel to the H-bridge circuit. The first SC cell is a combination of one capacitor, one diode and two switches (C_1-D_1-S_{11}-S_{12}), while the second SC cell includes one capacitor, one diode and three switches (C_2-D_2-S_{21}-S_{22}-S_{23}).

In the operation circuit, the C_1 capacitor is charged in parallel connection with the input source through S_{12}, while it is discharged in series connection with the input source through S_{11}. Also, the C_2 capacitor is charged in parallel connection with the C_1 capacitor, input source through S_{22} and anti-parallel diode of S_{23}, while it is discharged in series connection with the C_1 capacitor and input source through S_{21}, S_{23}.

Fig 3-2, Fig. 3-3 and Fig. 3-4 shows the nine operating states of the proposed SCMI. Fig. 3-5 describes the pulse-width modulation (PWM) scheme for the proposed SCMI. In the positive period, the circuit operation includes seven stages and four states [state 2 to state 5, Fig. 3-2 (b), Fig. 3-2(c), Fig. 3-3(a) and Fig. 3-3(b). In this period, the switches of the H-bridged is not changed, T_1 and T_4 are fully turned ON, while T_2 and T3 are fully turned OFF, the components of the SC cells are changed in each stage.

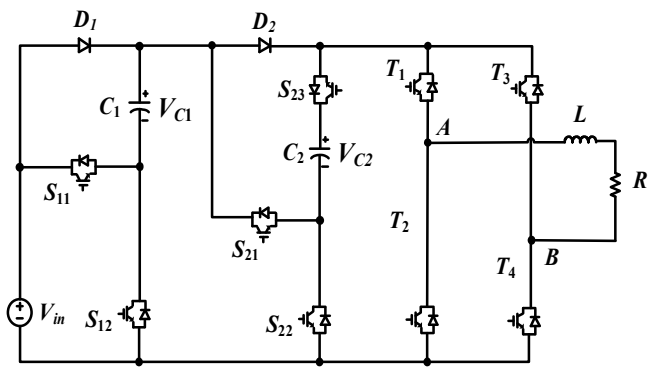
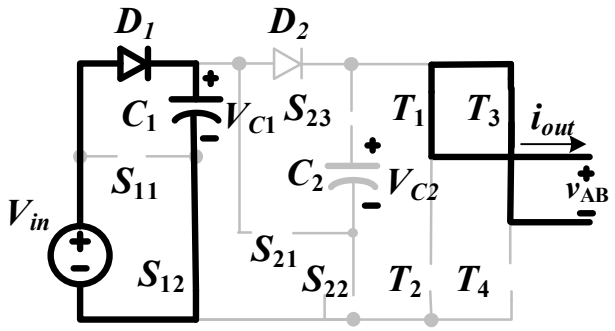
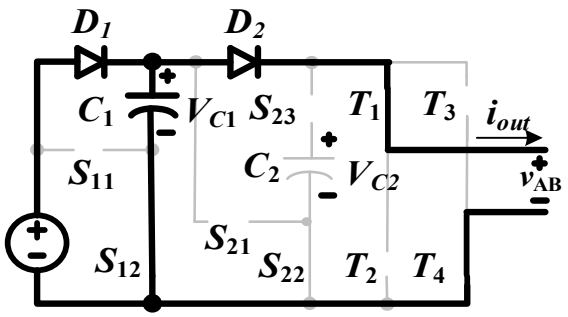


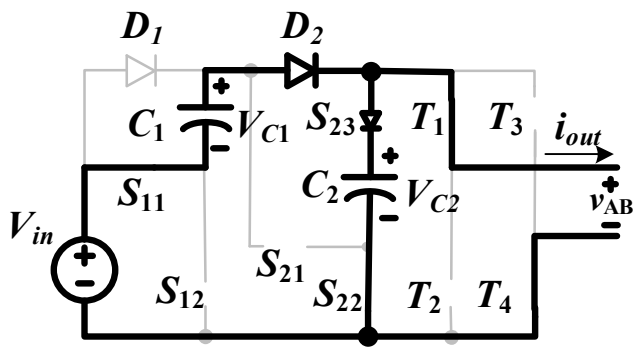
Fig. 3-1 Proposed SC nine-level inverter topology



(a) State 1

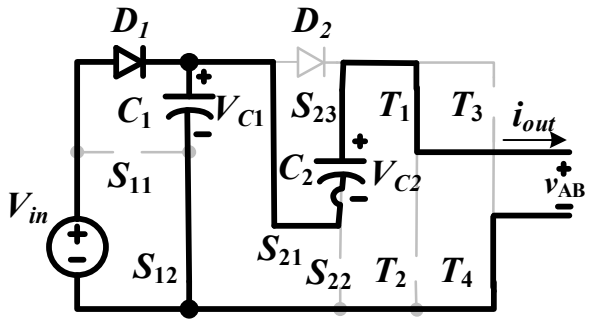


(b) State 2

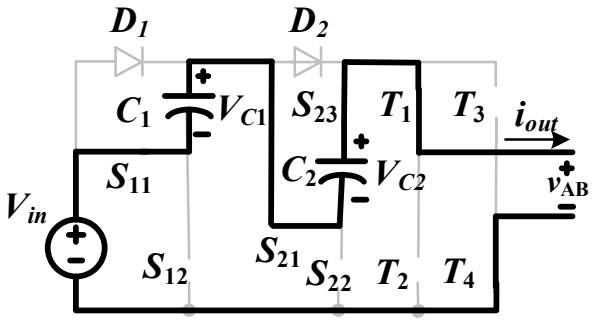


(c) State 3

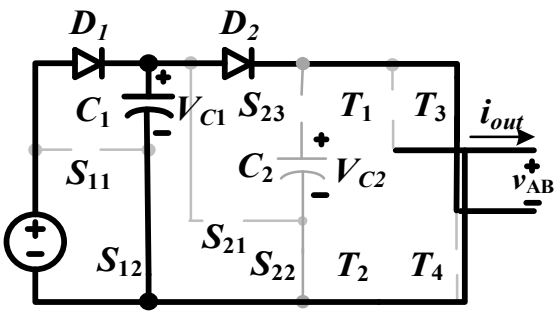
Fig. 3-2 Operation states and current flow of proposed SCMI



(a) State 4

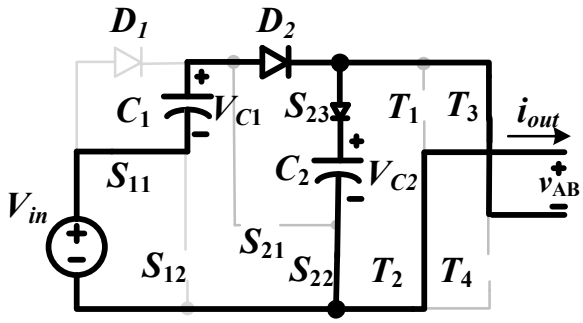


(b) State 5

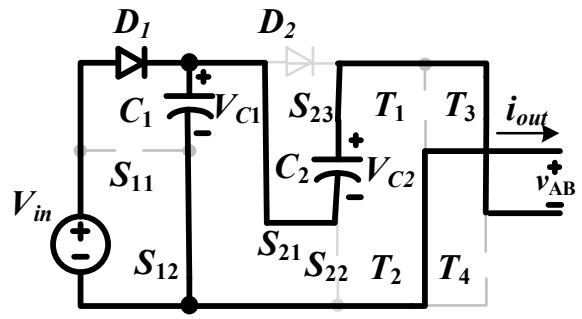


(c) State 6

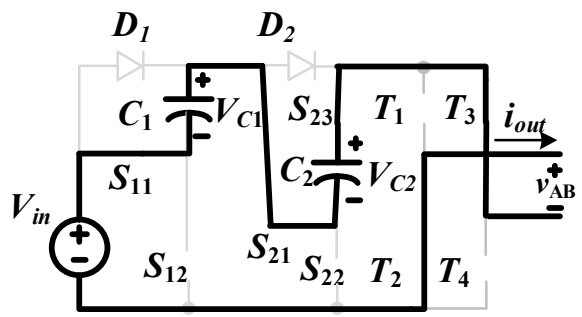
Fig. 3-3 Operation states and current flow of proposed SCMI



(a) State 7



(b) State 8



(c) State 9

Fig. 3-4 Operation states and current flow of proposed SCMI

Stage 1 - [t_0-t_1, Fig. 3-2(a) and Fig. 3-2(b)]: S_{12}, S_{22} and T_1 are fully turned ON, while S_{11}, S_{21}, S_{23} and T_2 are fully turned OFF. The D_1 diode is forward-biased. The C_1 capacitor is charged from the input voltage, and $V_{C1} = V_{in}$. If T_3 is turned ON and T_4 is turned OFF, the output voltage is zero ($V_{AB} = 0$) as shown in Fig. 3-2(a) for state 1. If T_3 is turned OFF and T_4 is turned ON, the output voltage is the input voltage ($V_{AB} = V_{in}$) as shown in Fig. 3-2(b) for state 2.

Stage 2 - [t_1-t_2, Fig. 3-2(b) and Fig. 3-2(c)]: S_{22} is fully turned ON, while S_{21} and S_{23} are fully turned OFF. The D_2 diode is forward-biased. If S_{11} is turned OFF and S_{12} is turned ON, the D_1 diode is forward-biased, the C_1 capacitor is charged from input voltage. The output voltage is $V_{AB} = V_{C1} = V_{in}$ as shown in Fig. 3-2(b) for state 2. If S_{11} is turned ON and S_{12} is turned OFF, the D_1 diode is reverse-biased, the C_1 capacitor is discharged while the C_2 capacitor is charged from input voltage and C_1 capacitor voltage, and $V_{C2} = V_{in} + V_{C1} = 2V_{in}$. The output voltage equals twice the input voltage ($V_{AB} = V_{C2} = 2V_{in}$) as shown in Fig. 3-2(c) for state 3.

Stage 3 - [t_2-t_3, Fig. 3-2(c) and Fig. 3-3(a)]: If S_{11} and S_{22} are turned ON and S_{12}, S_{21} and S_{23} are turned OFF, the D_1 diode is reverse-biased, the D_2 diode is forward-biased, the C_1 capacitor is discharged, while the C_2 capacitor is charged from input voltage and C_1 capacitor voltage. The output voltage is $V_{AB} = V_{in} + V_{C1} = 2V_{in}$ as shown in Fig. 3-2(c) for state 3. If S_{11} and S_{22} are turned OFF and S_{12}, S_{21} and S_{23} are turned ON, the D_1 diode is forward-biased, the D_2 diode is reverse-biased, the C_1 capacitor is charged from input voltage, while the C_2 capacitor is discharged, and the output voltage equals three times of the input voltage ($V_{AB} = V_{in} + V_{C2} = 3V_{in}$) as shown in Fig. 3-3(a) for state 4.

Stage 4 - [t_3-t_4, Fig. 3-3(a) and Fig. 3-3(b)]: S_{21} and S_{23} are fully turned ON, while S_{22} is fully turned OFF. The D_2 diode is reverse-biased, and the C_2 capacitor is discharged. If S_{12} is turned ON and S_{11} is turned OFF, the D_1

diode is forward-biased, the C_1 capacitor is charged from input voltage. The output voltage is $V_{AB} = V_{in} + V_{C2} = 3V_{in}$ as shown in Fig. 3-3(a) for state 4. If S_{12} is turned OFF and S_{11} is turned ON, the D_1 diode is reverse-biased, the C_1 capacitor is discharged; and the output voltage equals four times of the input voltage ($V_{AB} = V_{in} + V_{C1} + V_{C2} = 4V_{in}$) as shown in Fig. 3-3(b) for state 5.

Stage 5 - [t_4-t_5, Fig. 3-2(c) and Fig. 3-3(a)]: similar to the stage 3.

Stage 6 - [t_5-t_6, Fig. 3-2(b) and Fig. 3-2(c)]: similar to the stage 2.

Stage 7 - [t_6-t_7, Fig. 3-2(a) and Fig. 3-2(b)]: similar to the stage 1.

Similarly, in the negative period, the circuit operation includes seven stages with four states [state 6 to state 9 as shown in Fig. 3-3(c) and Fig. 3-4, respectively]. In this period, the switches of the H-bridge circuit are opposite with the positive period, T_2 and T_3 are fully turned ON, while T_1 and T_4 are fully turned OFF, the components of the SC cells are similar to the positive period in each stage. Table I sumarizes the operating states of the proposed SCMI.

Table 3-1 Switching States of the Proposed SCMI

No.	Case	State	On-state switches and diodes	VAB
1	$e_s > e_1$	5 (Fig. 3-3(b))	S_{11}, S_{21}, S_{23}, T_1, T_4.	$4V_{in}$
2	$e_1 \geq e_s > e_2$	4 (Fig. 3-3(a))	S_{12}, S_{21}, S_{23} T_1, T_4, D_1.	$3V_{in}$
3	$e_2 \geq e_s > e_3$	3 (Fig. 3-2(c))	S_{11}, S_{22}, T_1, T_4, D_2.	$2V_{in}$
4	$e_3 \geq e_s > e_4$	2 (Fig. 3-2(b))	S_{12}, S_{22}, T_1, T_4, D_1, D_2.	V_{in}
5	$e_4 \geq e_s > e_5$	1 (Fig. 3-2(a))	S_{12}, S_{22}, T_1, T_3, D_1, D_2.	0
6	$e_5 \geq e_s > e_6$	6 (Fig. 3-3(c))	S_{12}, S_{22}, T_2, T_3, D_1, D_2.	$-V_{in}$
7	$e_6 \geq e_s > e_7$	7 (Fig. 3-4(d))	S_{11}, S_{22}, T_2, T_3, D_2.	$-2V_{in}$
8	$e_7 \geq e_s > e_8$	8 (Fig. 3-4(b))	S_{12}, S_{21}, S_{23}. T_2, T_3, D_1.	$-3V_{in}$
9	$e_8 \geq e_s$	9 (Fig. 3-4(c))	S_{11}, S_{21}, S_{23}, T_2, T_3.	$-4V_{in}$

C. Proposed PWM Control Strategy

The PWM control strategies such as the space vector modulation (SVM) [27], [28], the phase disposition pulse-width modulation (PD-PWM) [29], the phase opposite disposition pulse width modulation (POD-PWM) [30], the alternative phase opposite disposition pulse-width modulation (APOD-PWM) [31], the selective harmonic elimination [27] and the hybrid modulation [32], can be used to control the SCMI. In this paper, the PD-PWM is used to control the proposed SCMI.

Fig. 3-5 shows the PD-PWM strategy of the proposed SCMI in a haft period. For nine-level inverter, eight carrier waveforms synchronized in the same phase and the same amplitude are used to control the switches. A reference waveform is $e_s = U_s*\sin(2\pi f_{ref})$, where f_{ref} and U_s are the frequency and the amplitude of the reference waveform, respectively. In the PD-PWM, the modulation index is determined by the ratio of the amplitude of the reference waveform and the carrier waveform.

For the proposed SCMI, the modulation coefficient is

$$M = \frac{U_s}{8U_c} \tag{1}$$

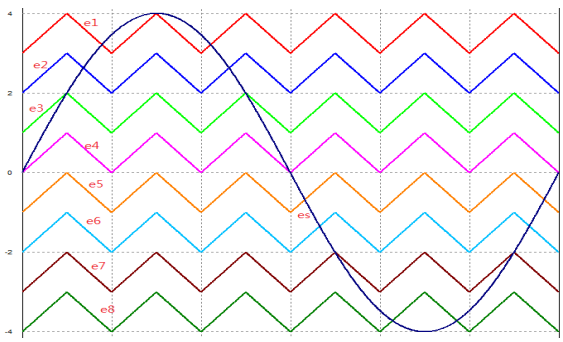


Fig. 3-5 The PD-PWM control strategy of the proposed SCMI

where U_S is the amplitude of the reference waveform, U_C is the amplitude of the carrier waveform.

The state of each switch depends on the comparison of the reference waveform value and the carrier waveforms value at a time. In Fig. 3-5, e_s is the reference waveform e_1, e_2, e_3 and e_4 are the carrier waveforms. The reference waveform (e_s) is compared with each carrier waveform e_1, e_2, e_3 and e_4 to generate the control signal on switches. All analysis results of control strategy are synthesized in Table 3.1.

Compared to other inverter configurations

The proposed SCMI is compared with three SCMI topologies in [18], [20] and [22]. Table 3.2 shows the number of voltage levels, switches, diodes, capacitors and sources for each topology. Under the same nine-level output voltage, the proposed SCMI has a lower the number of switches with a single source.

Table 3-2 Comparison with the Other Inverter Configurations

	Proposed SCMI	Inverter in [16]	Inverter in [18]	Inverter in [20]
The level number of inverter (n_{level})	9	9	9	9
The number of switches (n_{sw})	9	12	13	10
The number of diodes (n_D)	2	2	0	3
The number of capacitors (n_C)	2	2	3	3
The number of input sources (n_v)	1	2	1	1

Ⅳ. EXTEND PROPOSED SCMI

A. Introduction

The switched-capacitor nine-level inverter can be extended to the SC seventeen-level inverter by adding a SC cell include a capacitor, three semiconductor switches and one diodes (C_3-D_3-S_{31}-S_{32}-S_{33}), or extending to the SC thirty-three-level inverter by adding two SC cells. The proposed SCMI can be extended to the SC (2^{n+1}+1) level by adding n-SC cells.

B. Proposed Topology

Fig. 4-1 show the proposed SCMI with the SC (2^{n+1}+1) level by adding n-SC cells The operation principle of extended circuit topology is showed in Table III.

Based on the extend proposed SCMI, assuming the level number of the proposed SCMI is n_{level}, then the number of required semiconducting switches (n_{sw}), the number of capacitors (n_c), the number of power diodes (n_D) are calculated by the following equations:

$$\begin{bmatrix} n_{level} = 2^{nc+1} + 1 \\ n_{sw} = 3(n_c + 1) \\ n_c = \log_2(n_{level} - 1) - 1 \\ n_D = n_C \end{bmatrix} \quad (2)$$

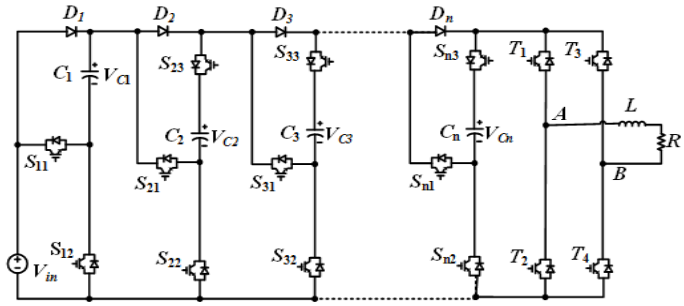


Fig. 4-1 Extended circuit topology of the proposoed SCMI

Table 4-1 Operation States of the Extend Proposed SCMI

No	On-state switches	VAB
1	S_{11}, S_{21}, ⋯, S_{n1} S_{23}, S_{33}, ⋯, S_{n3} T_1, T_4.	$(n+1)V_{in}$
2	S_{12}, S_{21}, S_{31}, ⋯, S_{n1} S_{23}, S_{33}, ⋯, S_{n3} T_1, T_4, D_1.	nV_{in}
3	S_{11}, S_{22}, S_{31}, S_{41}, ⋯, S_{n1} S_{33}, S_{43}, ⋯, S_{n3} T_1, T_4, D_2.	$(n-1)V_{in}$
4	S_{12}, S_{22}, S_{31}, S_{41}, ⋯, S_{n1} S_{33}, S_{43}, S_{53}, ⋯, S_{n3} T_1, T_4, D_1, D_2.	$(n-2)V_{in}$
⋯	⋯	⋯
$2^{n_c+1}-2$	S_{12}, S_{22}, S_{31}, S_{41}, ⋯, S_{n1} S_{33}, S_{43}, S_{53}, ⋯, S_{n3} T_2, T_3, D_1, D_2.	$(n-2)V_{in}$
$2^{n_c+1}-1$	S_{11}, S_{22}, S_{31}, S_{41}, ⋯, S_{n1} S_{33}, S_{43}, ⋯, S_{n3} T_2, T_3, D_2.	$(n-1)V_{in}$
2^{n_c+1}	S_{12}, S_{21}, S_{31}, ⋯, S_{n1} S_{23}, S_{33}, ⋯, S_{n3} T_2, T_3, D_1.	nV_{in}
$2^{n_c+1}+1$	S_{11}, S_{21}, ⋯, S_{n1} S_{23}, S_{33}, ⋯, S_{n3} T_2, T_3.	$(n+1)V_{in}$

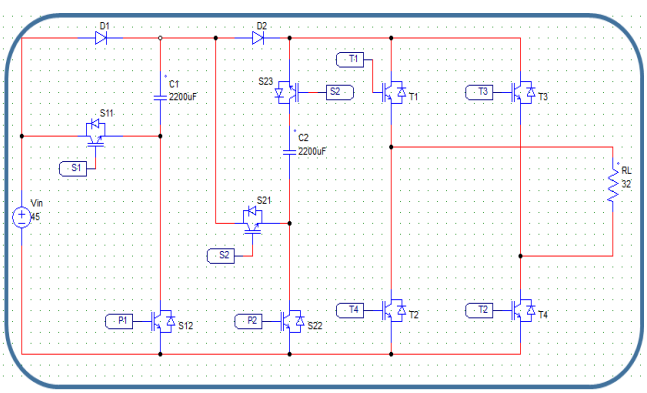
Ⅴ. Simulation and Experimental Results

A. Simulation results

To confirm the operation of the proposed SCMI, the simulation were performed for the proposed SCMI as shown in Fig. 5-1. The parameters of the proposed topology are chosen as listed in Table IV. Simulations were tested for both the resistive load (R = 80 Ω) and the inductive load (R = 80 Ω, L = 30 mH). The proposed SCMI produces 50-Hz sinusoidal voltage waveform with the desires output voltage of 122 V_{RMS}. The simulation was worked by PSIM 9.1 with the parameters is in Table 5.1.

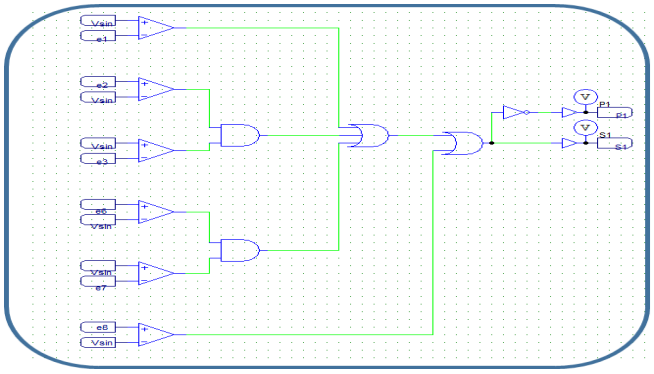
Table 5-1 Parameters For Simulation

Input voltage (V_{in})	48 V
Output voltage in RMS (V_{AB})	120 V
Capacitors (C_1 = C_2)	2200 μF
Carrier frequency (f_{car})	5 kHz
Output frequency (f_{ref})	50 Hz

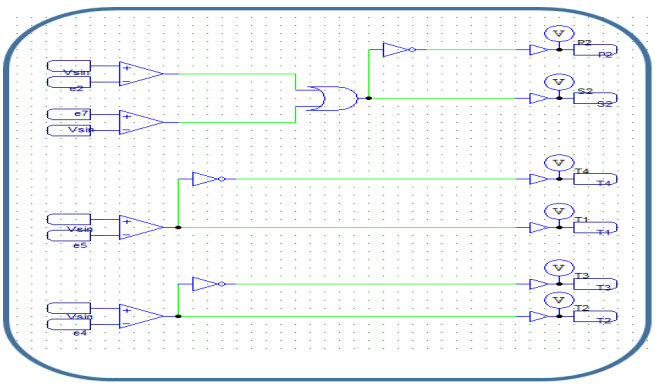


(a) Power circuit

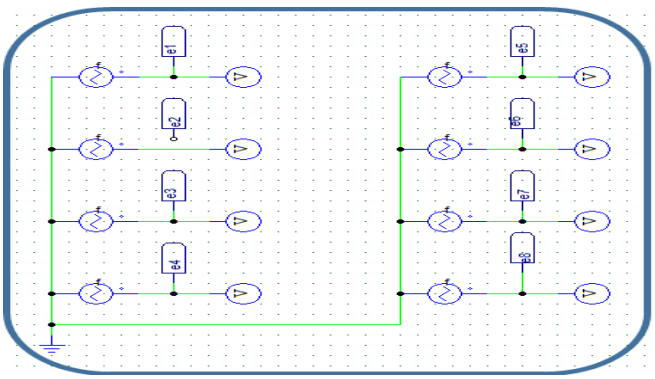
Fig. 5-1 PSIM schematic



(b) Control signal generation



(c) Control signal generation

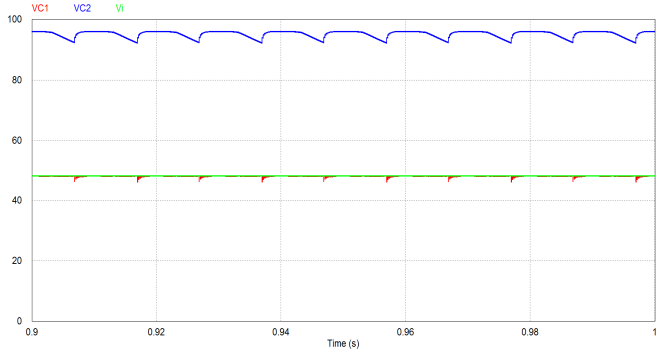


(d) Control signal generation

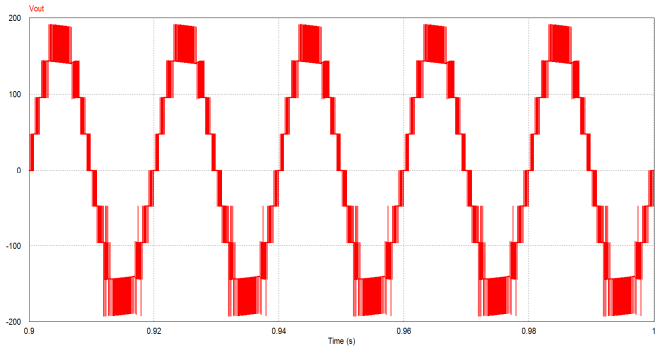
Fig. 5-1 (Continued from previous page)

1. Simulation results with high switching frequency (fs=5 KHz)

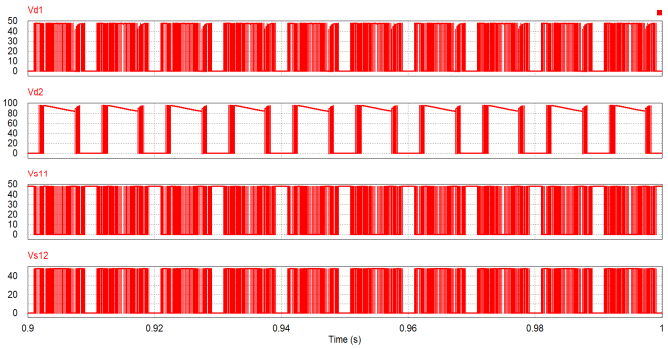
The switching frequency of the switches is 5 kHz. The Fig. 5-2 shows the simulation results with M = 3.6, the resistive load (R = 80 Ω). Fig. 5-2(a) shows the voltage waveform of the C_1 and C_2 capacitors. The maximum and minimum values of the C_1 capacitor voltage (V_{C1}) are 48 V and 46.2V, respectively. The maximum and minimum values of the C_2 capacitor voltage (V_{C2}) are 96 V and 92.3V, respectively. The output voltage waveform (V_o) has a nine-level stair waveform as shown in the Fig. 5-2(b) with the maximum voltage is 192 V from the input voltage is 48 Vdc. Fig. 5-2(c) shows the D_1, D_2 diodes voltage. The S_{11}-S_{12}-S_{21}-S_{22}-S_{23} switches voltage is discussed, as shown in Fig. 5-2(c),(d). The T_1 - T_4 switches voltage is shown in Fig. 5-2(e) to generate the voltage level of the output voltage.



(a) Input voltage, capacitors C_1 and C_2 voltage

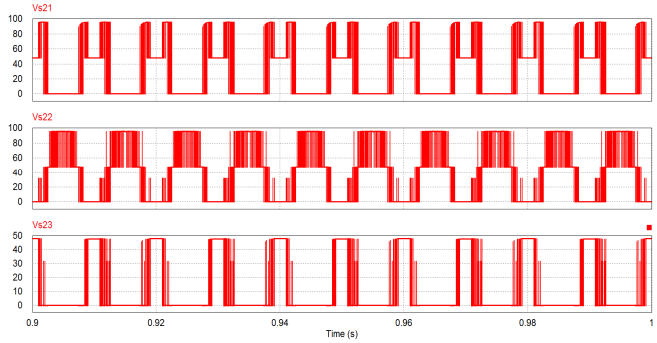


(b) Output voltage waveform(V_o) with the resistive load

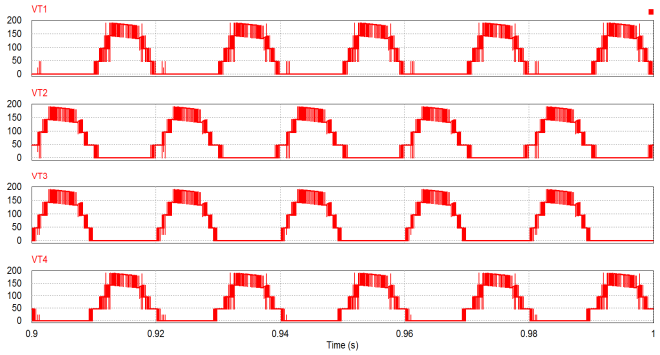


(c) Diodes D_1, D_2, switches S_{11} and S_{12} voltage

Fig. 5-2 Simulation results with resistive load R = 80 Ω and M = 3.6



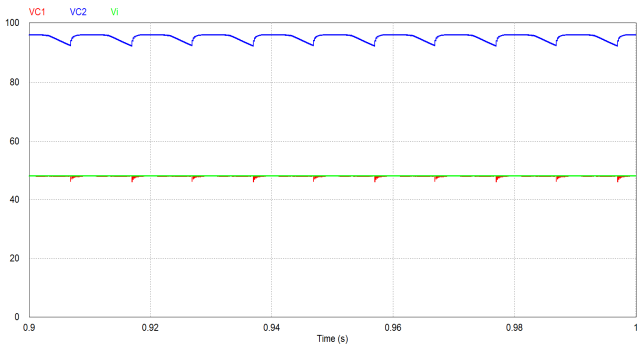
(d) Switches S_{21} - S_{23}, T_1 - T_4 voltage



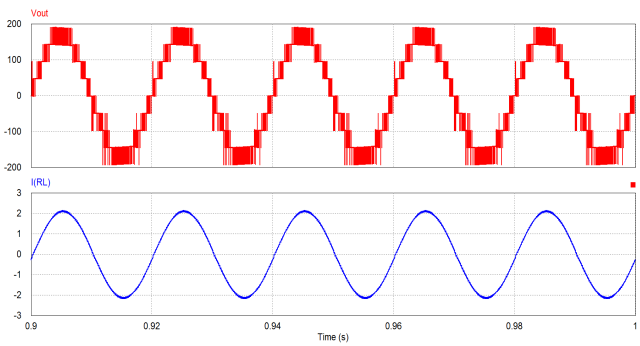
(e) Switches S_{21} - S_{23}, T_1 - T_4 voltage

Fig. 5-2 (Continued from previous page)

Fig. 5-3 shows the simulation results with M = 3.6, the inductive load (R = 80 Ω and L = 30 mH). The capacitors C_1 and C_2 voltage are 47.5 V and 95 V. The ripple voltage of the capacitors C_1 and C_2 are 1.5 V and 3.5 V, respectively. The load current lags the output voltage, the output and current voltage waveforms are shown in the Fig. 5-3(b). The output current waveform is shown in the Fig. 5-3(b) with the maximum current of 2.2 A. The other simulation voltage waveforms in case of the inductive load are similar with those in the resistive load in the Fig. 5-2.

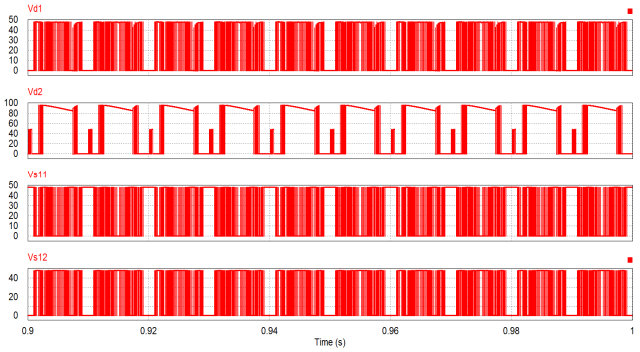


(a) Input voltage, capacitors C_1 and C_2 voltage

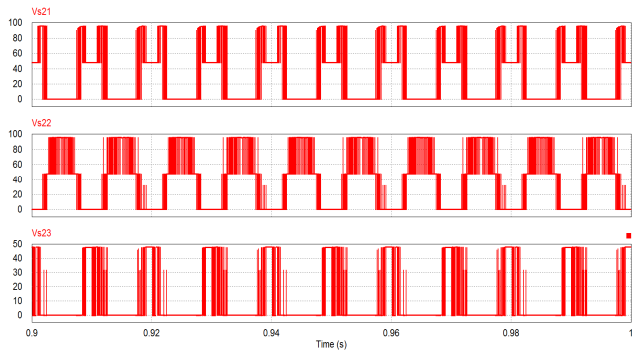


(b) Output voltage waveform (V_o) with the resistive load

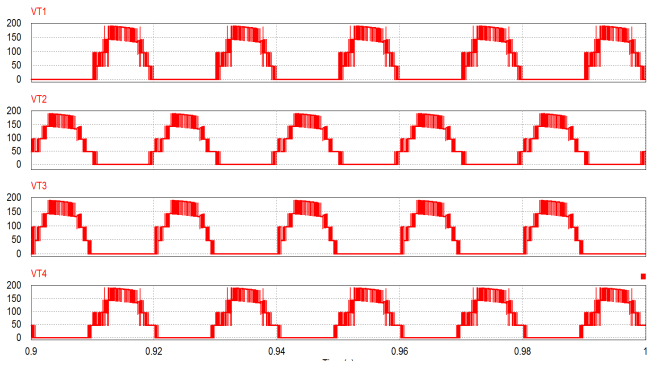
Fig. 5-3 Simulation results with M = 3.6, inductive load R = 80 Ω and Lo = 30 mH



(c) Diodes D_1, D_2, switches S_{11} and S_{12} voltage

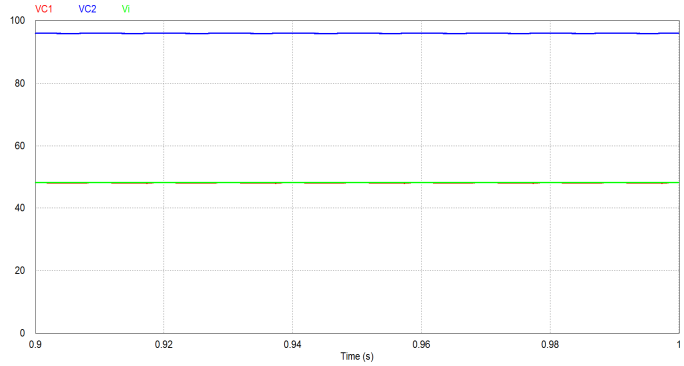


(d) Switches S_{21} - S_{23}, T_1 - T_4 voltage

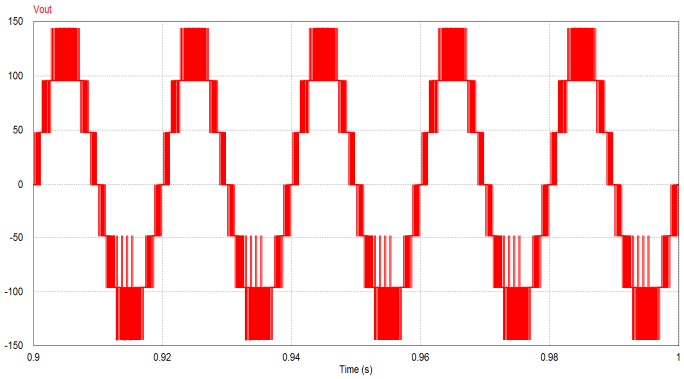


(e) Switches S_{21} - S_{23}, T_1 - T_4 voltage

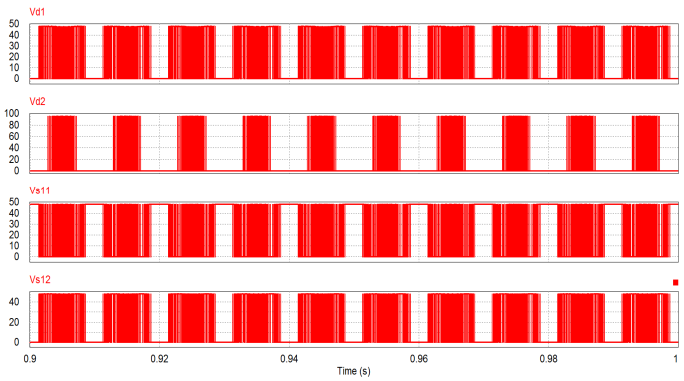
Fig. 5-3 (Continued from previous page)



(a) Input voltage, capacitors C_1 and C_2 voltage

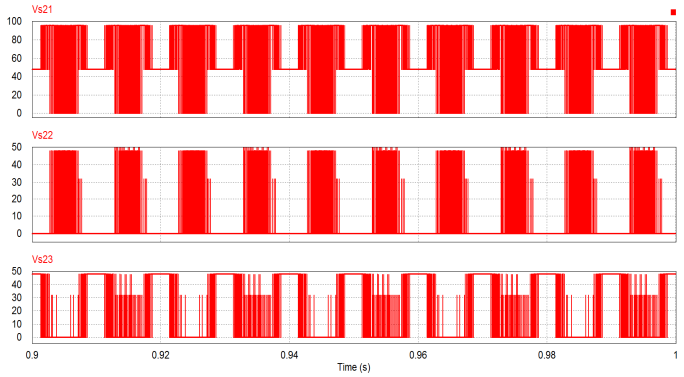


(b) Output voltage waveform (V_o) with the resistive load

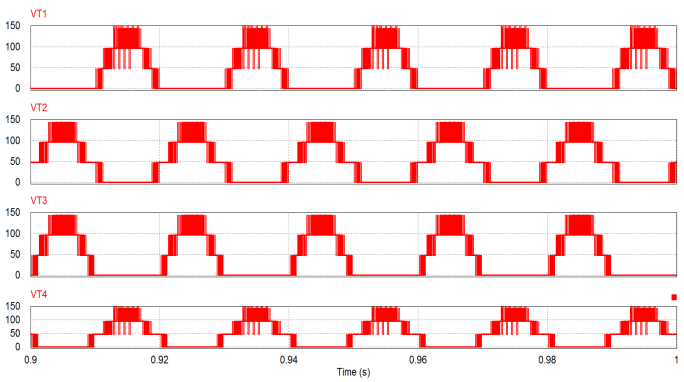


(c) Diodes D_1, D_2, switches S_{11} and S_{12} voltage

Fig. 5-4 Simulation results with resistive load R = 80 Ω and M = 2.6



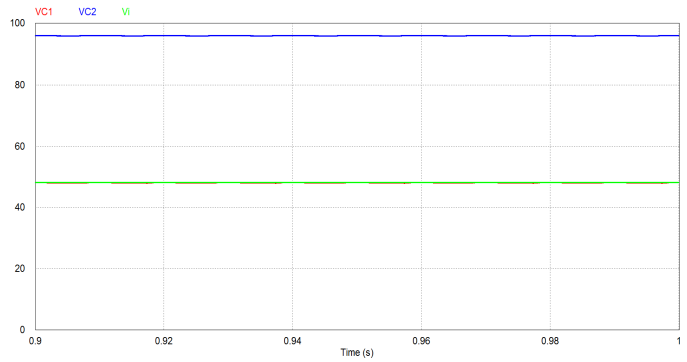
(d) Switches S_{21} - S_{23}, T_1 - T_4 voltage



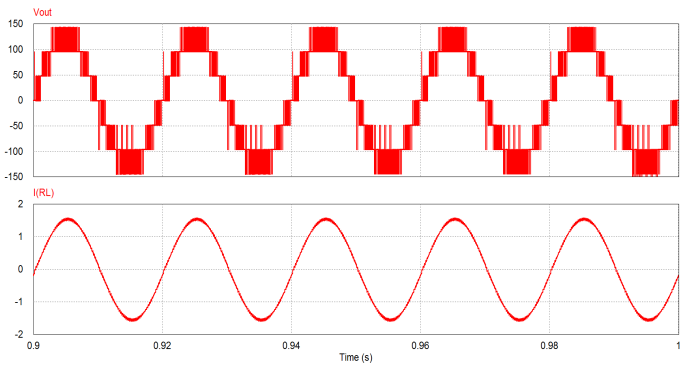
(e) Switches S_{21} - S_{23}, T_1 - T_4 voltage

Fig. 5-4 (Continued from previous page)

Fig. 5-4 shows the simulation results with the resistive load (R = 80 Ω) and inductive load (R = 80 Ω, L_o = 30 mH) but the modulation index is decreased to 2.6. The capacitors C_1 and C_2 voltage are 48 V and 96 V. The ripple voltage of the capacitors C_1 and C_2 are low with 0.5 V and 0.6 V, respectively. The output and current voltage waveforms are shown in the Fig. 5-5(b). The output voltage waveform (V_o) has a seven-level stair waveform as shown in the Fig. 5-4, 5-5(b). The output current waveform is shown in the Fig 5-5(d) with the maximum current of 1.6 A. The other simulation voltage waveforms in case of the inductive load are similar with those in the resistive load in the Fig. 5-4.

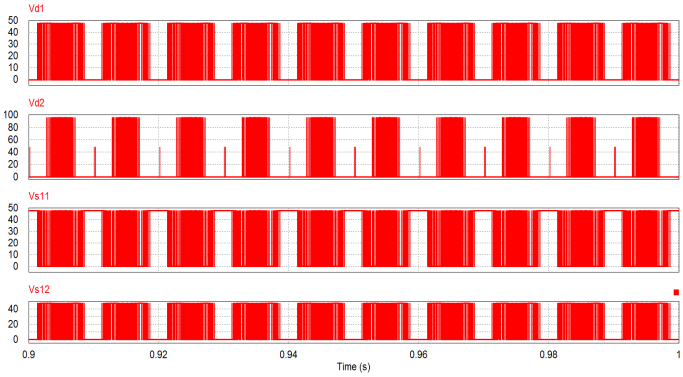


(a) Input voltage, capacitors C_1 and C_2 voltage

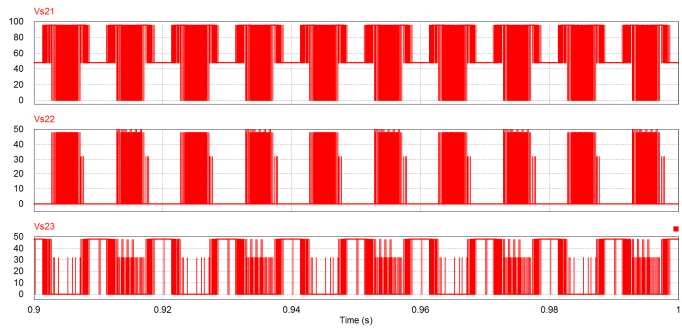


(b) Output voltage waveform (V_o) with the resistive load

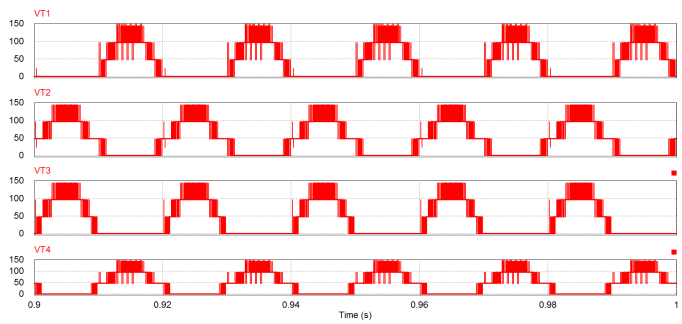
Fig. 5-5 Simulation results with M = 2.6, inductive load R = 80 Ω and L_o = 30 mH



(c) Diodes D_1, D_2, switches S_{11} and S_{12} voltage



(d) Switches S_{21} - S_{23}, T_1 - T_4 voltage

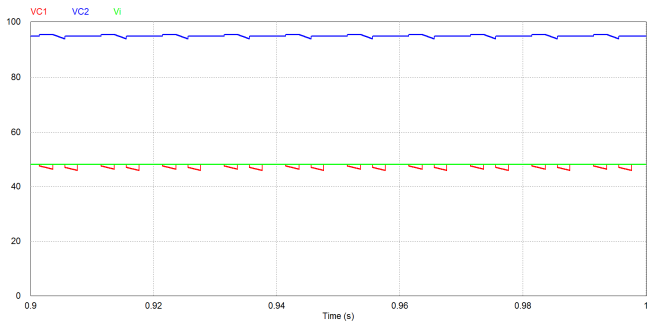


(e) Switches S_{21} - S_{23}, T_1 - T_4 voltage

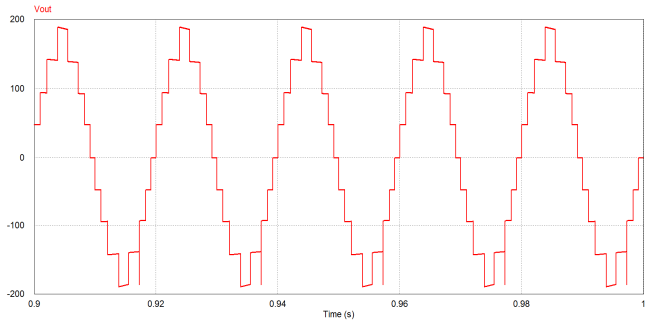
Fig. 5-5 (Continued from previous page)

2. Simulation results with low switching frequency (fs=50 Hz)

Fig. 5-6 shows the simulation results with M = 3.6 and the resistive load (R = 80 Ω) but the Carrier frequency is reduced into 50 Hz. The capacitors C_1 and C_2 voltage are 47.3 V and 93 V. The ripple voltage of the capacitors C_1 and C_2 are low with 4.5 V and 3.6 V, respectively. The output voltage waveform (V_o) has still a nine-level stair waveform as shown in the Fig. 5-6(b). The other simulation voltage waveforms in this case are similar with those in the resistive load in the Fig. 5-2 but the semiconductor devices are switching with the switching frequency of 50 Hz.

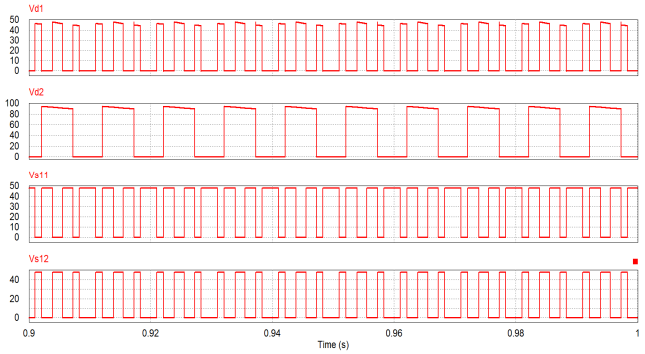


(a) Input voltage, capacitors C_1 and C_2 voltage

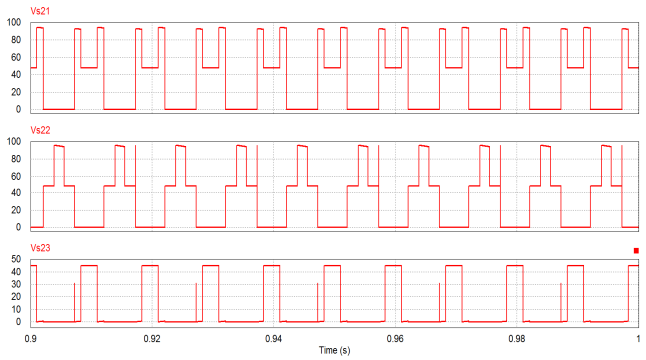


(b) Output voltage waveform (V_o) with the resistive load

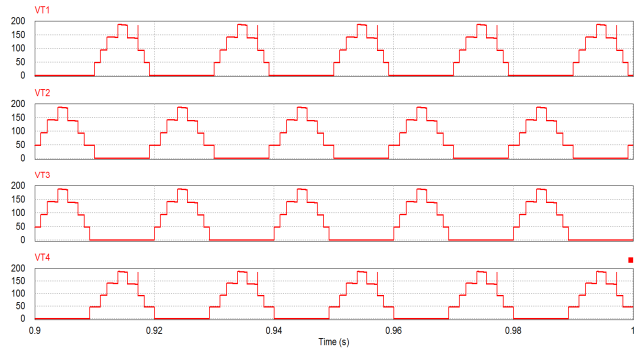
Fig. 5-6 Simulation results with M = 3.6, inductive load R = 80 Ω



(c) Diodes D_1, D_2, switches S_{11} and S_{12} voltage



(d) Switches S_{21} - S_{23}, T_1 - T_4 voltage



(e) Switches S_{21} - S_{23}, T_1 - T_4 voltage

Fig. 5-6 (Continued from previous page)

B. Experimental results

Based on the simulation results, the prototype of experiment was performed with the parameters in the Table 5.2. Fig. 5-7 shows experimental model of the proposed SCMI. To generate the PD-PWM scheme, the system used kit TMS320F28335 DSP of Texas Instruments and the PWM signals were created by the enhanced pulse width modulator (ePWM) module of the controller. All switches were G30N60 IGBTs with the low saturation voltage is 1.8 V, the maximum voltage and current stresses of 600 V and 30 A, respectively. All switches were driven by the isolated TLP250 amplifiers. Two power diodes DSEI30-60A were used with the forward voltage of 1.6 V, the maximum voltage and current stresses of 600 V and 37 A, respectively.

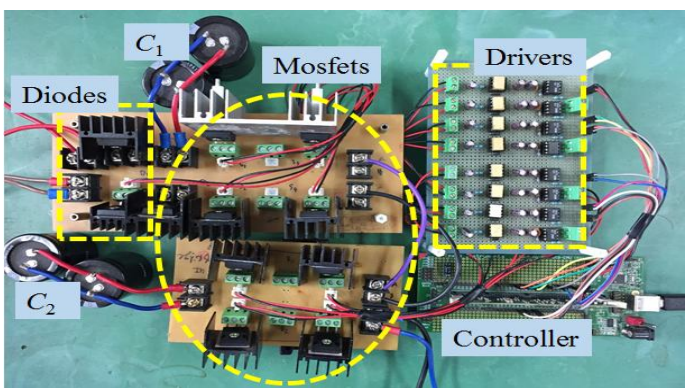


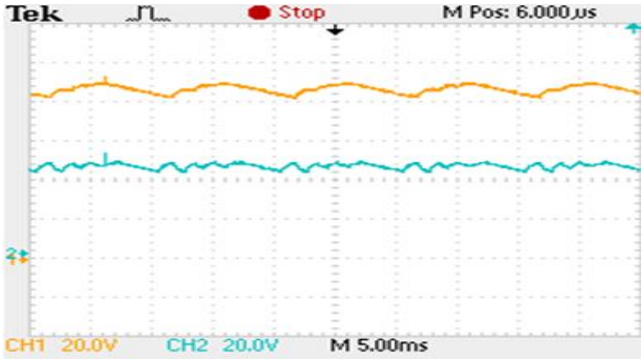
Fig. 5-7 Experimental model of the proposed SCMI

1. Experimental results with high switching frequency (fs=5KHz)

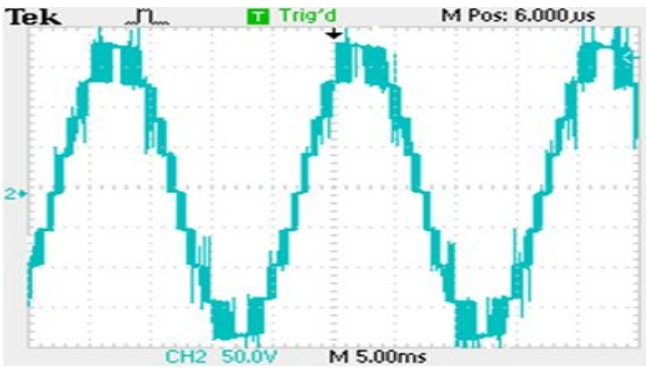
The switching frequency of the switches is 5kHz. Fig. 5-8 shows the experimental results with the resistive load (R = 80 Ω). Fig. 5-8(a) shows the voltage waveform of the C_1 and C_2 capacitors. The maximum and minimum capacitor C_1 voltages are 47.4V and 43V, respectively. So, the ripple voltage of C_1 is 4.4V. The maximum and minimum capacitor C_2 voltages are 90.4V and 84.7V, respectively. So, the ripple voltage of C_2 is 5.7V. Fig. 5-8(b) shows the output voltage waveform with nine-level. The total harmonic distortion(THD) of the proposed inverter is measured 11.7% as shown in Fig. 5-8(c). The output voltage is $120V_{RMS}$ with the frequency of 50Hz.

Table 5-2 Parameters For Experiment

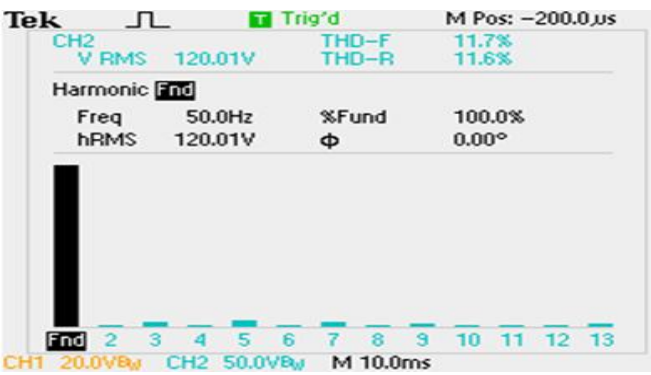
Input voltage (V_{in})	48 V
Output voltage in RMS (V_{AB})	120 V
Capacitors (C_1=C_2)	2200 μF/ 200 V
Carrier frequency (f_{car})	5 kHz
Output frequency (f)	50 Hz
IGBTs	G30N60 (600 V, 60 A, V_{CE}=1.8V)
Diodes	DSEI30-06A (600 V, 37 A, V_F=1.6V)
Load (L_f)	80 Ω for resistive load 80 Ω and 30 mH for passive load



(a) Capacitor C_1 and C_2 voltage



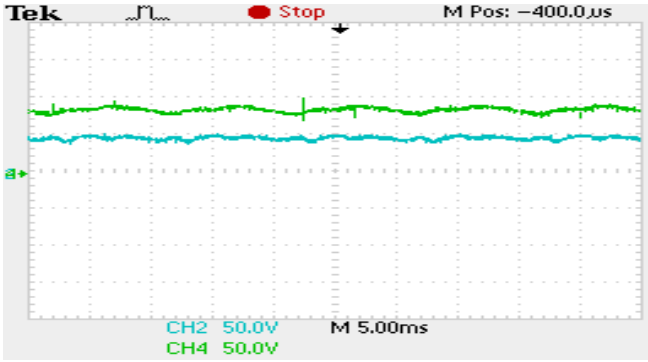
(b) Output voltage(V_{AB})



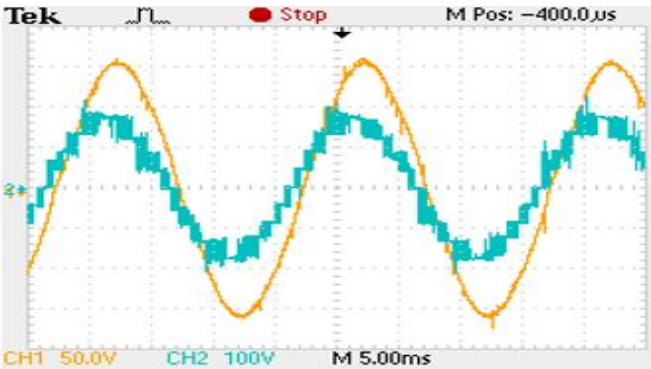
(c) Harmonics of output voltage

Fig. 5-8 Experimental results with the resistive load (R = 80 Ω)

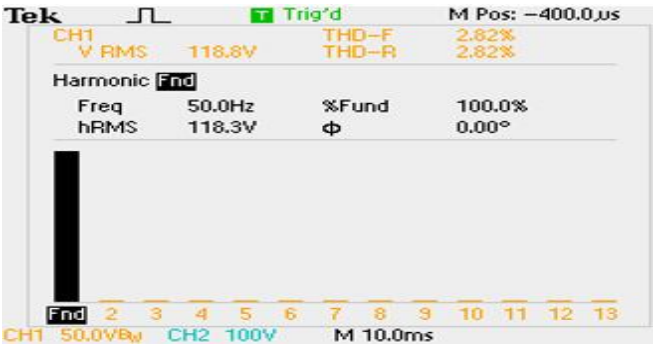
Fig. 5-9 shows the experimental results with the inductive load. Fig. 5-9(a) shows the voltage waveform of the C_1 and C_2 capacitors. The maximum and minimum capacitor C_1 voltages are 48V and 41V, respectively. So, the ripple voltage of C_1 is 7V. The maximum and minimum capacitor C_2 voltages are 96V and 83.7V, respectively. So, the ripple voltage of C_2 is 12.3V. Fig. 5-9(b) shows the output voltage waveform with nine-level. The total harmonic distortion(THD) of the output voltage and load Rvoltage are measured 2.8% and 10.7% as shown in Fig. 5-9(c) and Fig. 5-9(d), respectively. The output voltage is 120VRMS with the frequency of 50Hz. And output current is $1.5A_{RMS}$ with the frequency of 50Hz.



(a) Capacitors C_1 and C_2 voltage

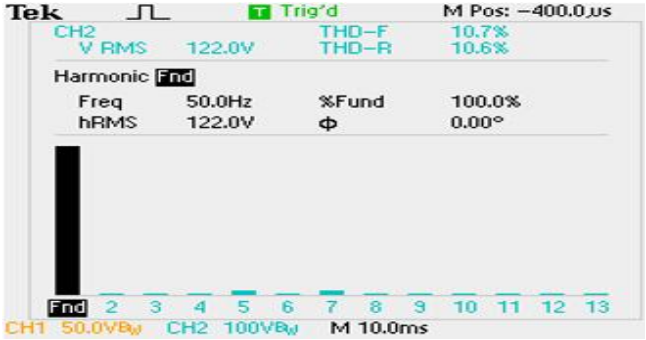


(b) Output voltage waveforms (V_{AB} and V_R)

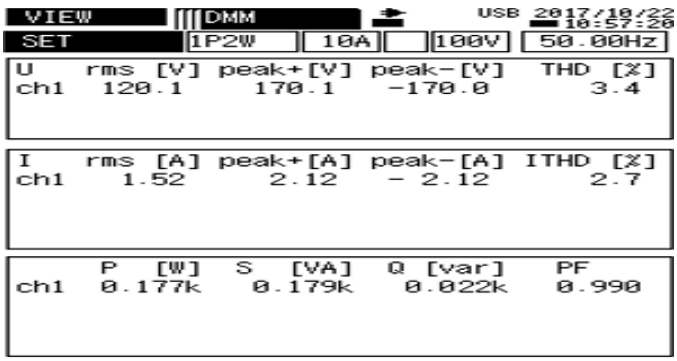


(c) Harmonics of voltage waveform on resistor and output voltage and the output power

Fig. 5-9 Experimental results with inductive load (R = 80 Ω, L = 30 mH)



(d) Harmonics of voltage waveform on resistor and output voltage and the output power



(e) Harmonics of voltage waveform on resistor and output voltage and the output power

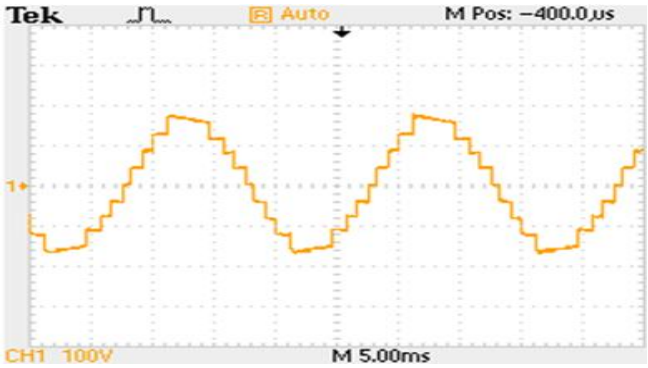
Fig. 5-9 (Continued from previous page)

2. Experimental results with low switching frequency (f_s=50Hz)

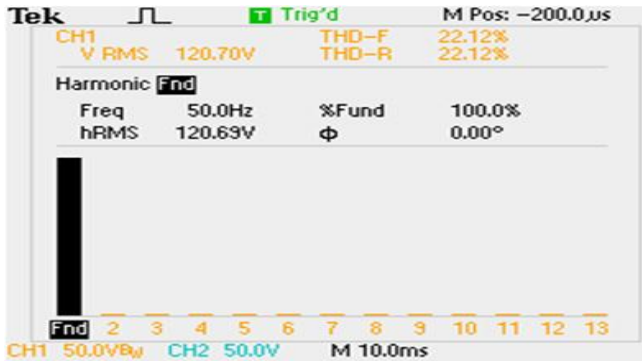
The switching frequency of the switches is reduced from 5kHz to 50Hz. Fig. 5-10 and Fig. 5-11 show the experimental results with the low switching frequency.

Fig. 5-10 shows the resistive load (R = 80 Ω). Fig. 5-10(a) shows the output voltage waveform with nine-level. The total harmonic distortion (THD) of the proposed inverter is measured 22.1 % as shown in Fig. 5-10(b). The output voltage is 120 V_{RMS} with the frequency of 50Hz.

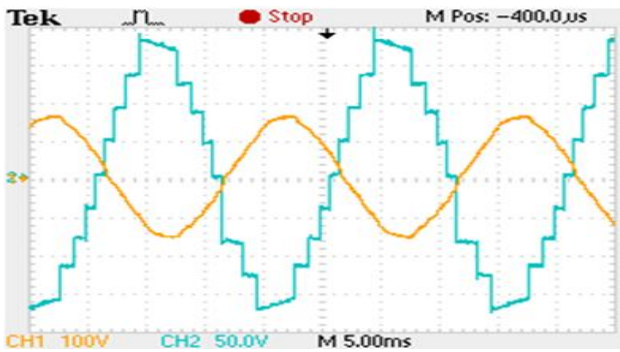
Fig. 5-11 shows the experimental results with the inductive load (R = 80 Ω and L = 30 mH). The voltage on resistor (V_R) has a phase angle with the output voltage (V_{AB}). The measured THD value of load voltage is 22.4 %. And, the measured THD value of V_R is 5.1 %.



(a) Output voltage waveform

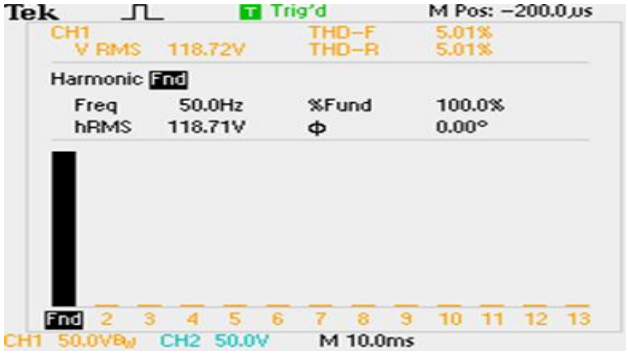


(b) Harmonics of output voltage waveform

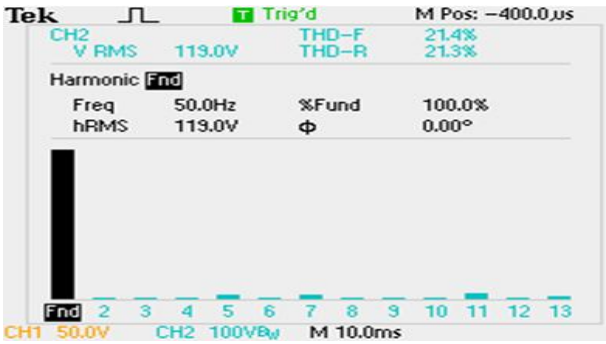


(a) Output voltage waveforms (V_{AB} and V_R)

Fig. 5-10 Experimental results with resistive load (R = 80 Ω)



(b) Harmonics of voltage waveform on resistor



(c) Harmonics of output voltage waveform

Fig. 5-11 Experimental results with passive load (R = 80 Ω, L = 30 mH)

Ⅵ. Conclusions

This thesis research has been focused on switched-capacitor multi level inverter. The main conclusions from this research are summarized below:

1- A new switched-capacitor multi level inverter (SCMI) topology has been proposed. The proposed SCMI has a lower number of components than the traditional MIs. By switching the capacitor in series and in parallel, the output voltage is larger than the input voltage with self-balanced capacitors.

2- The extension of the proposed SCMI was proposed. By adding n-SC cells, the proposed SCMI can be extended to the SC ($2^{n+1}+1$) level

In addition, the PWM modulation method of the proposed SC nine-level inverter were shown. A steady-state circuit analysis and the operational stages in the proposed SC nine-level inverter have been described. In order to verify the performance of the proposed converter, the laboratory prototype based on TMS320F2812 DSP and PSIM simulation have been performed. The simulation and the experimental results with both a resistive load R and a passive load RL have been showed.

The calculations for the determine of capacitance and the loss calculation have been done.

Contributions made in this dissertation are:

- Power circuit design and implementation;
- Development of new topology for the multi level inverter;
- Development of control algorithm for the proposed SC nine-level inverter;
- Solutions to issues on digital implementations are provided

References

[1] Chavarria J., Biel D., Guinjoan F., Meza C., and Negroni J. J.: 'Energy balance control of PV cascaded multi level grid-connected inverters under level-shifted and phase-shifted PWMs', IEEE Trans. Ind. Electron., 2013, 60, (1), pp. 98 - 111.

[2] Kouro S., Malinowski M., Gopakumar K., Pou J., Franquelo G. L., Wu B., Rodriguez J., Perez M., and Leon J.: 'Recent advances and industrial applications of multi level converters', IEEE Trans. Ind. Electron., 2010, 57, (8), pp. 2553 - 2580.

[3] Buticchi G., Lorenzani E., and Franceschini G.: 'A five-level single-phase grid-connected converter for renewable distributed systems', IEEE Trans. Ind. Electron., 2013, 60, (3), pp. 906 - 918.

[4] Ajami A., Oskuee M. R. J., Mokhberdoran A., and Bossche A. V.: 'Developed cascaded multi level inverter topology to minimise the number of circuit devices and voltage stresses of switches', IET Power Electron., 2014, 7, (2), pp. 459 - 466.

[5] Nabae A., Takahashi I., and Akagi H.: 'A new neutral-point-clamped PWM inverter', IEEE Trans. Ind. Appl., 1981, IA-17, (5), pp. 518 - 523.

[6] Rodriguez J., Bernet S., Steimer P. K., and Lizama I. E.: 'A survey on neutral-point-clamped inverters', IEEE Trans. Ind. Electron., 2010, 57, (7), pp. 2219 - 2230.

[7] Bina M. T., Firouz Y., and Eskandari B.: 'Efficiency of three-level neutral-point clamped converters: analysis and experimental validation of power losses, thermal modelling and lifetime prediction', IET Power Electron., 2014, 7, (1), pp.209 - 219.

[8] E. Ozdemir, S. Ozdemir, and L. M. Tolbert, "Fundamental-frequency modulated six-level diode-clamped multi level inverter for three-phase

standalone photovoltaic system," IEEE Trans. Ind. Electron., 2009, 56, (11), pp. 4407 - 4415.

[9] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "multi level SVPWM with DC-link capacitor voltage balancing control for diode-clamped multi level converter based STATCOM," IEEE Trans. Ind. Electron., 2013, 60, (5), pp. 1884 - 1896.

[10] A. K. Sadigh, V. Dargahi, and K. A. Corzine, "Analytical determination of conduction and switching power losses in flying-capacitor-based active neutral-point-clamped multi level converter," IEEE Trans. Power Electron., 2016, 31, (8), pp. 5473 - 5494.

[11] Kou X., Corzine K. A., and Familiant Y. L.: 'A unique fault-tolerant design for flying capacitor multi level inverter', IEEE Trans. Power Electron., 2004, 19, (4), pp. 979 - 987.

[12] Khazraei M., Sepahvand H., Corzine K. A., and Ferdowsi M.: 'Active capacitor voltage balancing in single-phase flying-capacitor multi level power converters', IEEE Trans. Ind. Electron., 2012, 59, (2), pp. 769 - 778.

[13] Dargahi S., Babaei E., Eskandari S., and Sabahi M.: 'Flying-capacitor stacked multicell multi level voltage source inverters: analysis and modelling', IET Power Electron., 2012, 7, (12), pp. 2929 - 2987.

[14] Druant J., Vyncke T., Belie F. D., Sergeant P., and Melkebeek J.: 'Adding inverter fault detection to model-based predictive control for flying-capacitor inverters', IEEE Trans. Ind. Electron., 2015, 62, (4), pp. 2054 - 2063.

[15] P. Roshankumar, P. P. Rajeevan, K. K.Mathew, J. I. Gopakumar, and L. G. Leon, "A five-level inverter topology with single dc supply by cascading a flying capacitor inverter and an H-bridge," IEEE Trans. Power Electron., 2012, 27, (8), pp. 3505 - 3512.

[16] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, “Double flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation,” IEEE Trans. Power Electron., 2010, 25, (6), pp. 1517 - 1526.

[17] J. Mathew, P. P. Rajeevan, K. Mathew, N. A. Azeez, and K. Gopakumar, “A multi level inverter scheme with dodecagonal voltage space vectors based on flying capacitor topology for induction motor drives,” IEEE Trans. Power Electron., 2013, 28, (1), pp. 516 - 525.

[18] V. Dargahi, A. K. Sadigh, M. Abarzadeh, S. Eskandari, and K. Corzine, “A new family of modular multi level converter based on modified flying capacitor multicell converters,” IEEE Trans. Power Electron., 2015, 30, (1), pp. 138 - 147.

[19] Rodríguez J., Lai J. S., and Peng F. Z.: ‘multi level inverters: A survey of topologies, controls, and applications’, IEEE Trans. Ind. Electron., 2002, 49, (4), pp. 724 - 738.

[20] Malinowski M., Gopakumar K., Rodriguez J., and Perez M. A.: ‘A survey on cascaded multi level inverters’, IEEE Trans. Ind. Electron., 2010,57, (7), pp. 2197 - 2206.

[21] Ghazanfari A., Mokhtari H., and Firouzi M.: ‘Simple voltage balancing approach for CHB multi level inverter considering low harmonic content based on a hybrid optimal modulation strategy’, IEEE Trans. Power Del., 2012, 27, (4), pp. 2150 - 2158.

[22] Fazel S. S., Bernet S., Krug D., and Jalili K.: ‘Design and comparison of 4-kv neutral-point-clamped, flying-capacitor, and series-connected H-bridge multi level converters’, IEEE Trans. Ind. Appl., 2007, 43, (4), pp. 1032-1040.

[23] Orfanoudakis G. I., Yuratich M. A., and Sharkh S. M.: ‘Analysis of dc-link capacitor current in three-level neutral point clamped and

cascaded H-bridge inverters', IET Power Electron., 2013, 6, (7), pp. 1376 - 1389.

[24] Liu J., Sun Y., Li Y., Fu C.: 'Theoretical harmonic analysis of cascaded H-bridge inverter under hybrid pulse width multi level modulation', IET Power Electron., 2016, 9, (14), pp. 2714 - 2722.

[25] Sirisukprasert S., Huang A. Q., and Lai J-S, 'Analysis and control of cascaded-multi level converter-based STATCOM', Power Engineering Society General Meeting., 2003, 4, pp. 2561-2568.

[26] Ding, K., Cheng, K.W.E., Zou, Y.P.: 'Analysis of an asymmetric modulation methods for cascaded multi level inverters', IET Power Electron., 2012, 5, (1), pp. 74 - 85.

[27] Villanueva E., Correa P., Rodríguez J., and Pacas M ,' Control of a single-phase cascaded H-bridge multi level inverter for grid-connected photovoltaic systems', IEEE Trans. Ind. Electron., 2009, 56, (11), pp. 4399 - 4406.

[28] Zha X., Xiong L., Gong J. and Liu F.: 'Cascaded multi level converter for medium-voltage motor drive capable of regenerating with part of cells', IET Power Electron., 2014, 7, (5), pp. 1313 - 1320.

[29] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energybalance control of PV cascaded multi level grid-connected inverters under level-shifted and phase-shifted PWMs," IEEE Trans. Ind. Electron., 2013, 60, (1), pp. 98 - 111.

[30] M. F. Kangarlu and E. Babaei, "A generalized cascaded multi level inverter using series connection of submulti level inverters," IEEE Trans. Power Electron., 2013, 28, (2), pp. 625 - 636.

[31] E. Babaei and S. S. Gowgani, "Hybrid multi level Inverter Using Switched Capacitor Units," IEEE Trans. Ind. Electronics., vol. 61, no. 9, pp. 4614-4621, Sep. 2014.

[32] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/ parallel conversion with inductive load," IEEE Trans. Ind. Electron., vol 59, no 2, pp. 878 - 887, Feb. 2012.

[33] Pradeep. K. P, and Vivek. A: 'Photovoltaic module-integrated stand-alone single-stage switched capacitor inverter with maximum power point tracking', IEEE Trans. Power Electron., 2017, 32, (5), pp. 3571 - 3584.

[34] Ebrahim. B, and Saeed. S. G: 'Hybrid multi level inverter using switched capacitor units', IEEE Trans. Ind. Electron., 2014, 61, (9), pp. 4614 - 4621.

[35] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," IEEE Trans. Ind. Electron., 2011,58, (6), pp. 2435 - 2443.

[36] C. M. Young, N. Y. Chu, Y. C. Hsiao, and C. Z. Li, "A single-phase multi level inverter with battery balancing," IEEE Trans. Ind. Electron., 2013, 60, (5), pp. 1972 - 1978.

[37] E. Babaei, "Optimal topologies for cascaded sub-multi level converters," J. Power Electron., 2010, 10, (3), pp. 251 - 261.

[38] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space-vector pulsewidth modulation for three-level NPC converter with the neutral point voltage control," IEEE Trans. Ind. Electron., 2011, 58, (11), pp. 5076 - 5086.

[39] V. G. Agelidis, A. I. Balouktsis, and C. Cossar, "On attaining the multiple solutions of selective harmonic elimination PWM three-level waveforms through function minimization," IEEE Trans. Ind. Electron., 2008, 55, (3), pp. 996 - 1004.

[40] Amir. T, Jafar. A, and Mohammad. R, "A self-balanced step-up multi level inverter based on switched-capacitor structure" IEEE Trans. Power Electron., 2018, 33, (1), pp. 199 - 209.

[41] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, “multi level converters for large electric drives,” IEEE Trans. Ind. Appl., 1999, 35, (1), pp. 36 - 44.

[42] Y. H. Chang, “Design and analysis of multistage multiphase switched capacitor boost DC - AC inverter,” IEEE Trans. Circuits Syst. I, 2011, 58, (1), pp. 205 - 218.

[43] F. Z. Peng, “A generalized multi level inverter topology with self voltage balancing,” IEEE Trans. Ind. Appl., 2001, 37, (2), pp. 611 - 618.

[44] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, “A step-up switched-capacitor multi level inverter with self voltage balancing,” IEEE Trans. Ind. Electron., 2014, 61, (12), pp. 6672 - 6680.

[45] Y. Liu and F. L. Luo, “multi level inverter with the ability of self-voltage balancing,” IEE Proc. Elect. Power Appl., 2006, 153, (1), pp. 105 - 115.

[46] M. S. W. Chan and K. T. Chau, “A new switched-capacitor boost multi level inverter using partial charging,” IEEE Trans. Circuits Syst. II, Express Briefs, 2007, (54), 12, pp. 1145 - 1149.

[47] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, “multi level inverter topologies with reduced device count: A review,” IEEE Trans. Power Electron., 2015, 31, (1), pp. 135 - 151.

[48] R. Barzegarkhoo, H. M. Kojabadi1, E. Zamiry, N. Vosooghi, and L. Chang, “Generalized structure for a single phase switched-capacitor multi level inverter using a new multiple DC link producer with reduced number of switches,” IEEE Trans. Power Electron., 2016, 31, (8), pp. 5604 - 5617.

[49] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, “A new cascaded switched-capacitor multi level inverter based on improved series - parallel conversion with less number of

components," IEEE Trans. Ind. Electron., 2016, 63, (6), pp. 3582 - 3594.

[50] C.-K. Cheung, S.-C. Tan, C. Tse, and A. Ioinovici, "On energy efficiency of switched-capacitor converters," IEEE Trans. Power Electron., 2013, 28, (2), pp. 862 - 876.

[51] M. Evzelman and S. Ben-Yaakov, "Average-current-based conduction losses model of switched capacitor converters," IEEE Trans. Power Electron., 2013, 28, (7), pp. 3341 - 3352.

[52] Barzegarkhoo R., Kojabadi H. M., Zamiry E., Vosooghi N., and Chang L.: 'Generalized structure for a single phase switched-capacitor multi level inverter using a new multiple dc link producer with reduced number of switches', IEEE Trans. Power Electron., 2016, 31, (8), pp. 5604 - 5617.

[53] Liu H., Tolbert L. M., Khomfoi S., Ozpineci B., and Du Z.: 'Hybrid cascaded multi level inverter with PWM control method', IEEE Power Electron. Spec. Conf., 2008, pp. 162 - 166.

[54] Liu J., Cheng K. W. E., and Ye Y.: 'A cascaded multi level inverter based on switched-capacitor for high-frequency ac power distribution system', IEEE Trans. Power Electron., 2014, 29, (8), pp. 4219-4230.

[55] Hinago Y., and Koizumi H.: 'A switched-capacitor inverter using series/ parallel conversion', IEEE Int. Symp. Circuits Syst., 2010, pp. 3188 - 3191.

[56] Hinago Y., and Koizumi H.: 'A switched-capacitor inverter using series/parallel conversion with inductive load', IEEE Trans. Ind. Electron., 2012, 59, (2), pp. 878-887.

[57] Kalashani M. B., and Farsadi M.: 'A new switched-capacitors boost inverter for renewable energy sources and POD control modulation', Electrical Engineering (ICEE)., 2014 22nd Iranian Conference on, pp. 636-641.

[58] Babaei E., and Gowgani S. S.: 'Hybrid multi level inverter using switched capacitor units', IEEE Trans. Ind. Electron., 2014, 61, (9), pp. 4614-4621.

[59] Tsunoda A., Hinago Y., and Koizumi H.: 'Level- and phase-shifted PWM for seven-level switched-capacitor inverter using series/parallel conversion', IEEE Trans. Ind. Electron., 2014, 61, (8), pp, 4011-4021.

[60] Mak O. C., and Ioinovici A.: 'Switched-capacitor inverter with high power density and enhanced regulation capability', IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., 1998, 45, (4), pp. 336 - 347.

[61] Saha B., and Kim R. Y.: 'High power density series resonant inverter using an auxiliary switched capacitor cell for induction heating applications', IEEE Trans. Power Electron., 2014, 29, (4), pp. 1909-1918.

[62] Li D., Loh P. C., Zhu M., Gao F., and Blaabjerg F.: 'Generalised multicell switched-inductor and switched-capacitor Z-source inverters', IEEE Trans. Power Electron., 2013, 28, (2), pp. 837-848.

[63] Ahmed J., and Borghate V. B.: 'Simplified space vector modulation technique for seven-level cascaded H-bridge inverter', IET Power Electron., 2014, 7, (3), pp. 604 - 613.

[64] Ma M., He X., Cao W., Song X., and Ji B.: 'Optimised phase disposition pulse-width modulation strategy for hybrid-clamped multi level inverters using switching state sequences', IET Power Electron., 2015, 8, (7), pp. 1095-1103.

[65] Shi X., Wang Z., Tolbert L., and Wang F.: 'A comparison of phase disposition and phase shift PWM strategies for modular multi level converters', Proc. IEEE Energy Convers. Congr. Expo., 2013, pp. 4089-4096.

[66] McGrath B. P., and Grahame D.: 'Multicarrier PWM strategies for multi level inverter', IEEE transaction on industrial electronics., 49, (4), pp. 858

- 867.

[67] Mazumder S. K.: 'Hybrid modulation scheme for a high frequency ac link inverter', IEEE Trans. Power. Electron., 2016, 31, (1), pp. 861 - 870.

[68] Fei W., Du X. and Wu B.: 'A Generalized Half - Wave Symmetry SHE-PWM Formulation for multi level Voltage Inverters', IEEE Trans. on Industrial Electronics, Vol. 57, No. 9, Sept. 2010.